7477/7478 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 7477/7478 group is the single-chip microcomputer designed with CMOS silicon gate technology.

The single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

In addition, built-in PROM type microcomputers with built-in electrically writable PROM, and additional functions equivalent to the mask ROM version are also available.

7477/7478 group products are shown noted below.

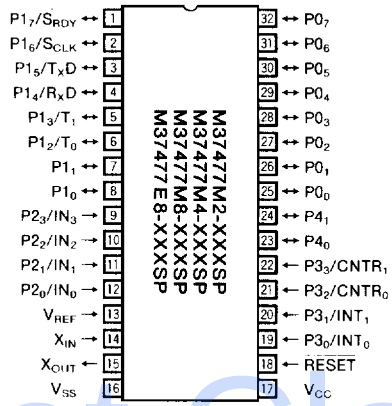
The 7477 and the 7478 differ in the number of I/O ports, package outline, and clock generating circuit only.

Product	Version
M37477M2-XXXSP/FP	Mask ROM version
M37477M4-XXXSP/FP	
M37477M8-XXXSP/FP	
M37477E8SP/FP	One Time PROM version (Built-in PROM type microcomputers)
M37477E8-XXXSP/FP	
M37478M2-XXXSP/FP	Mask ROM version
M37478M4-XXXSP/FP	
M37478M8-XXXSP/FP	
M37478E8SP/FP	One Time PROM version (Built-in PROM type microcomputers)
M37478E8-XXXSP/FP	
M37478E8SS	PROM version (Built-in PROM type microcomputer)

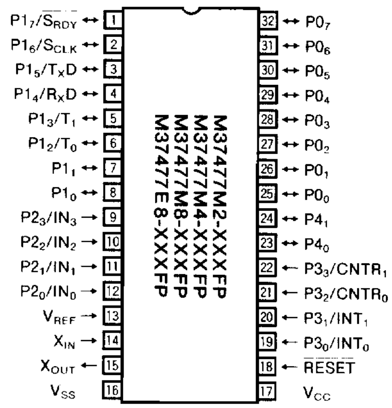
FEATURES

- Number of basic instructions 71
- Memory size
  ROM .... 4096 bytes (M37477M2,M37478M2)
  RAM .... 128 bytes (M37477M2,M37478M2)
- The minimum instruction execution time
  .... 0.5μs (at 8MHz oscillation frequency)
- Power source voltage
  .... 2.7 to 5.5V (at 4MHz oscillation frequency)
  4.5 to 5.5V (at 8MHz oscillation frequency)
- Power dissipation in normal mode
  .... 35mW (at 8MHz oscillation frequency)
- Subroutine nesting
  .... 64 levels max. (M37477M2, M37478M2)
- Interrupt 13types, 11vectors
- 8-bit timers 4
- Programmable I/O ports
  (Ports P0, P1, P4) 18 (M37477)
  20 (M37478)
- Input ports (Ports P2, P3) 8 (M37477)
  (Ports P2, P3, P5) 16 (M37478)
- 8-bit serial I/O .... 1 (UART or clock-synchronized)
- 8-bit A-D converter .... 4 channels (M37477)
  8 channels (M37478)

PIN CONFIGURATION (TOP VIEW)



Outline 32P4B



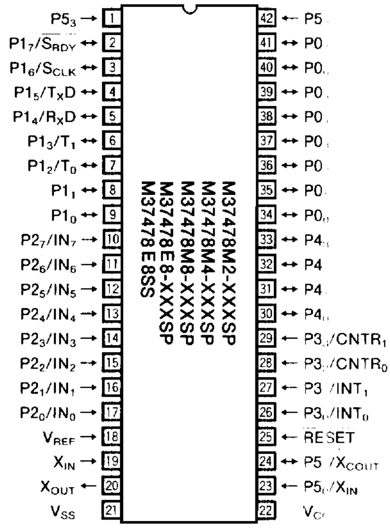
Outline 32P2W-A

APPLICATION

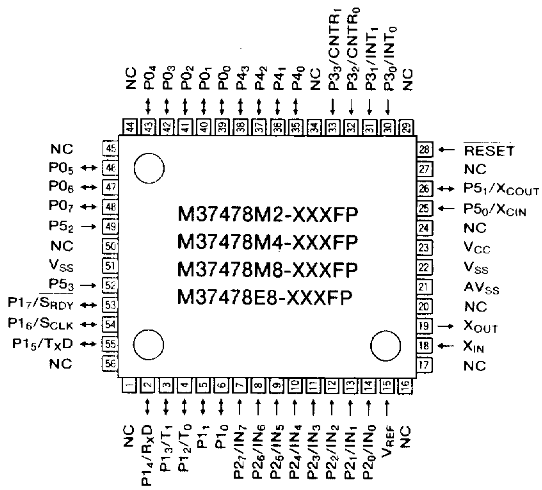
Audio-visual equipment, VCR, Tuner, Office automation equipment

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)



Outline 42P4B
42S1B-A (Window)

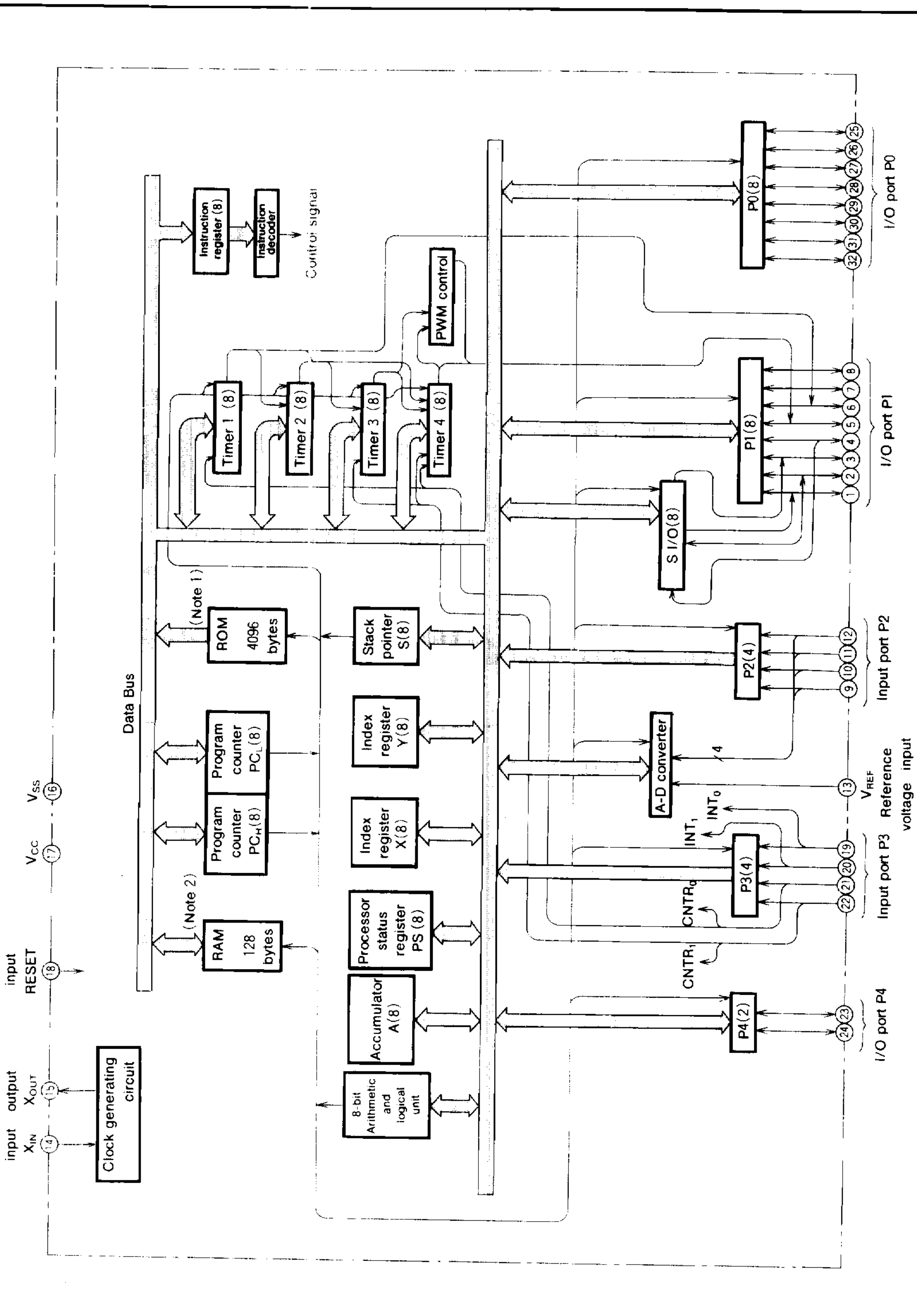


Outline 56P6N-A

Note. The differences between 42P4B package type of 7478 group and 56P6N-A package type of 7478 group are package outline, power dissipation ability (absolute maximum ratings), and the provision of an AV_{SS} pin by the 56P6N-A package type.

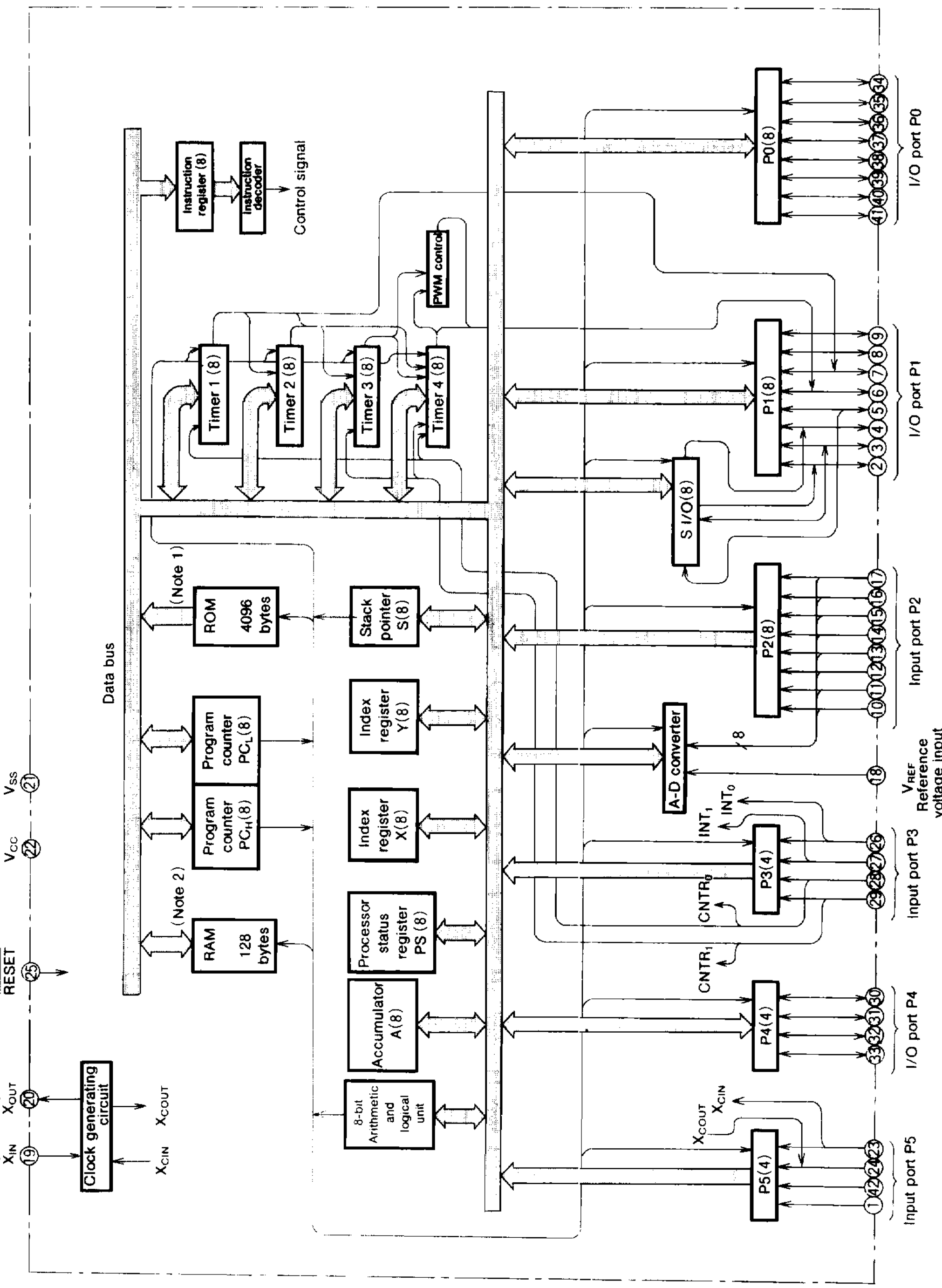
NC : No connection

M37477M2-XXXSP/FP BLOCK DIAGRAM

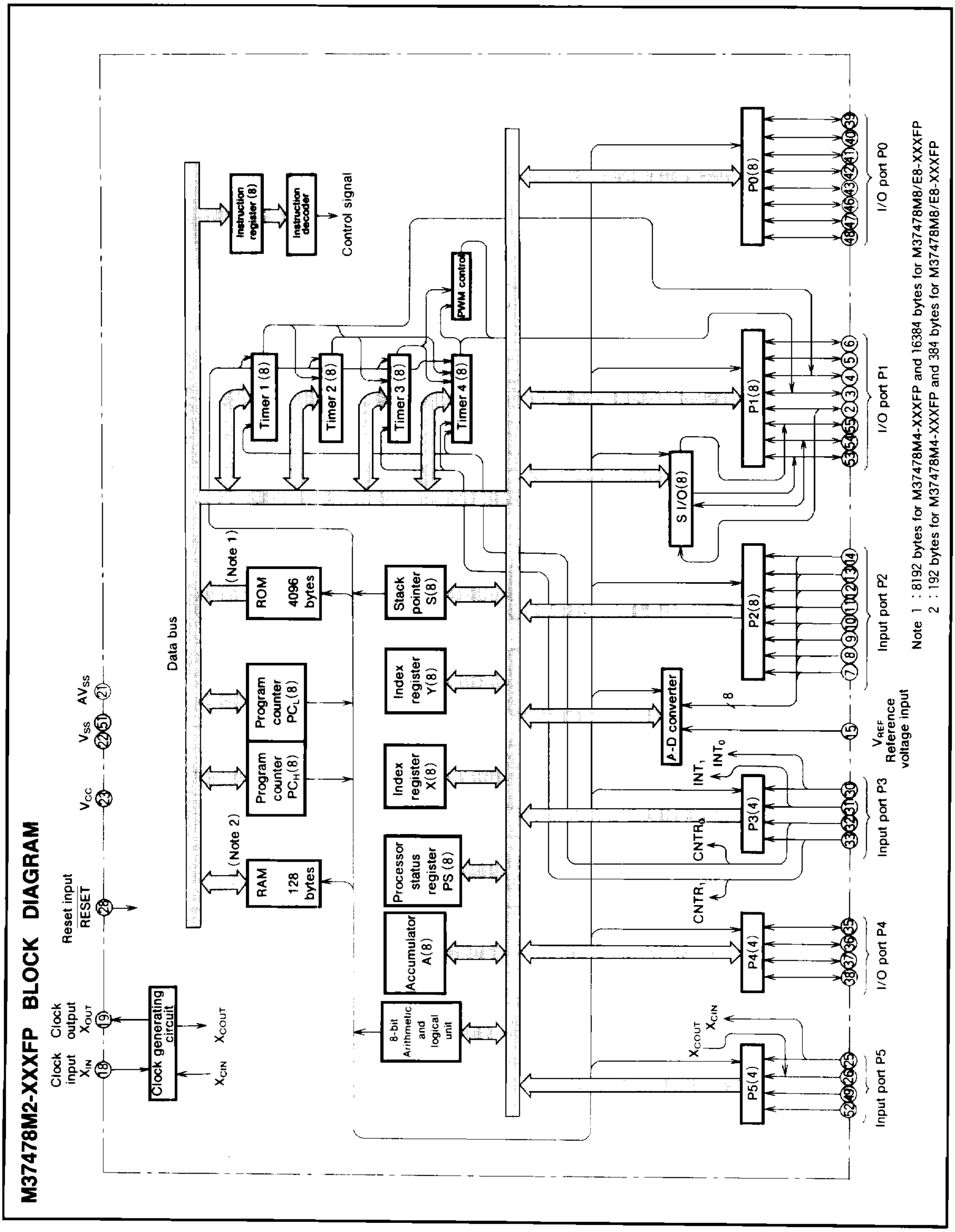


Note 1 : 8192 bytes for M37477M4-XXXSP/FP and 16384 bytes for M37477M8/E8-XXXSP/FP
2 : 192 bytes for M37477M4-XXXSP/FP and 384 bytes for M37477M8/E8-XXXSP/FP

M37478M2-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37478M4-XXXSP and 16384 bytes for M37478M8/E8-XXXSP, M37478E8SS
2 : 192 bytes for M37478M4-XXXSP and 384 bytes for M37478M8/E8-XXXSP, M37478E8SS



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FUNCTIONS OF 7477/7478 GROUP

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5μs (The minimum instructions, at 8MHz oscillation frequency)
Clock frequency			8MHz (max.)
Memory size	M37477M2	ROM	4096 bytes
	M37478M2	RAM	128 bytes
	M37477M4	ROM	8192 bytes
	M37478M4	RAM	192 bytes
	M37477M8/E8	(P)ROM	16384 bytes
	M37478M8/E8	RAM	384 bytes
Input/Output port	P0, P1	I/O	8-bit×2
	P2	Input	8-bit×1 (4-bit×1 for the M37477)
	P3, P5	Input	4-bit×2 (Port P5 is not included in the M37477)
	P4	I/O	4-bit×1 (2-bit×1 for the M37477)
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (8 channels) (8-bit×1 (4 channels) for the M37477)
Subroutine nesting	M37477M2, M37478M2		64 (max.)
	M37477M4, M37478M4		96 (max.)
	M37477M8/E8, M37478M8/E8		192 (max.)
Interrupt			5 external interrupts, 7 internal interrupts, 1 software interrupt
Clock generating circuit			Built-in circuit with internal feedback resistor (a ceramic or a quartz-crystal oscillator)
Power source voltage			2.7 to 5.5V (at 4MHz oscillation frequency), 4.5 to 5.5V (at 8MHz oscillation frequency)
Power dissipation			35mW (at 8MHz oscillation frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		−5 to 10mA (P0, P1, P4 : CMOS tri-states)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37477M2/M4/M8/E8-XXXSP		32-pin shrink plastic molded DIP
	M37477M2/M4/M8/E8-XXXFP		32-pin plastic molded SOP
	M37478M2/M4/M8/E8-XXXSP		42-pin shrink plastic molded DIP
	M37478M2/M4/M8/E8-XXXFP		56-pin plastic molded QFP
	M37478E8SS		42-pin ceramic DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source		Apply voltage of 2.7 to 5.5V to V_{CC}, and 0V to V_{SS}.
AV_{SS}	Analog power source		Ground level input pin for A-D converter. Same voltage as V_{SS} is applied. This pin is for M37478M2/M4/M8/E8-XXXFP only.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at "L" for 2μs or more (under normal V_{CC} conditions).
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D converter.
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided.
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1. $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins R_XD, T_XD, S_{CLK}, $\overline{S_{RDY}}$, respectively.
$P2_0$—$P2_7$ (Note 1)	Input port P2	Input	Port P2 is an 8-bit input port. This port is in common with analog input pins IN_0—IN_7.
$P3_0$—$P3_3$	Input port P3	Input	Port P3 is a 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
$P4_0$—$P4_3$ (Note 2)	I/O port P4	I/O	Port P4 is a 4-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
$P5_0$—$P5_3$ (Note 3)	Input port P5	Input	Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT}. If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin. Feedback resistor is connected between X_{CIN} and X_{COUT} pins.

Note 1 : Only $P2_0$—$P2_3$ (IN_0—IN_3) 4-bit for the 7477 group.
2 : Only $P4_0$ and $P4_1$ 2-bit for the 7477 group.
3 : This port is not included in the 7477 group

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)
The 7477/7478 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 〈Software〉 User's Manual for details on the instruction set.
Machine-resident 740 family instructions are as follows:
The FST and SLW instruction cannot be used.
The MUL, DIV, WIT, and STP instruction can be used.

CPU Mode Register
The CPU mode register is allocated at address $00FB_{16}$. This register contains the stack page selection bit.

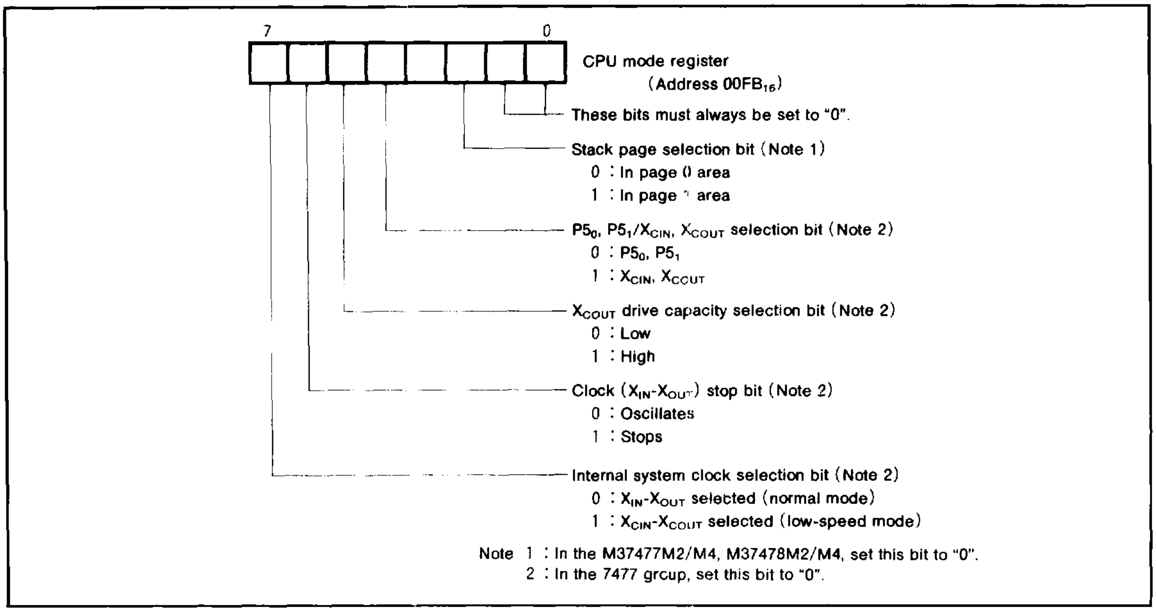


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

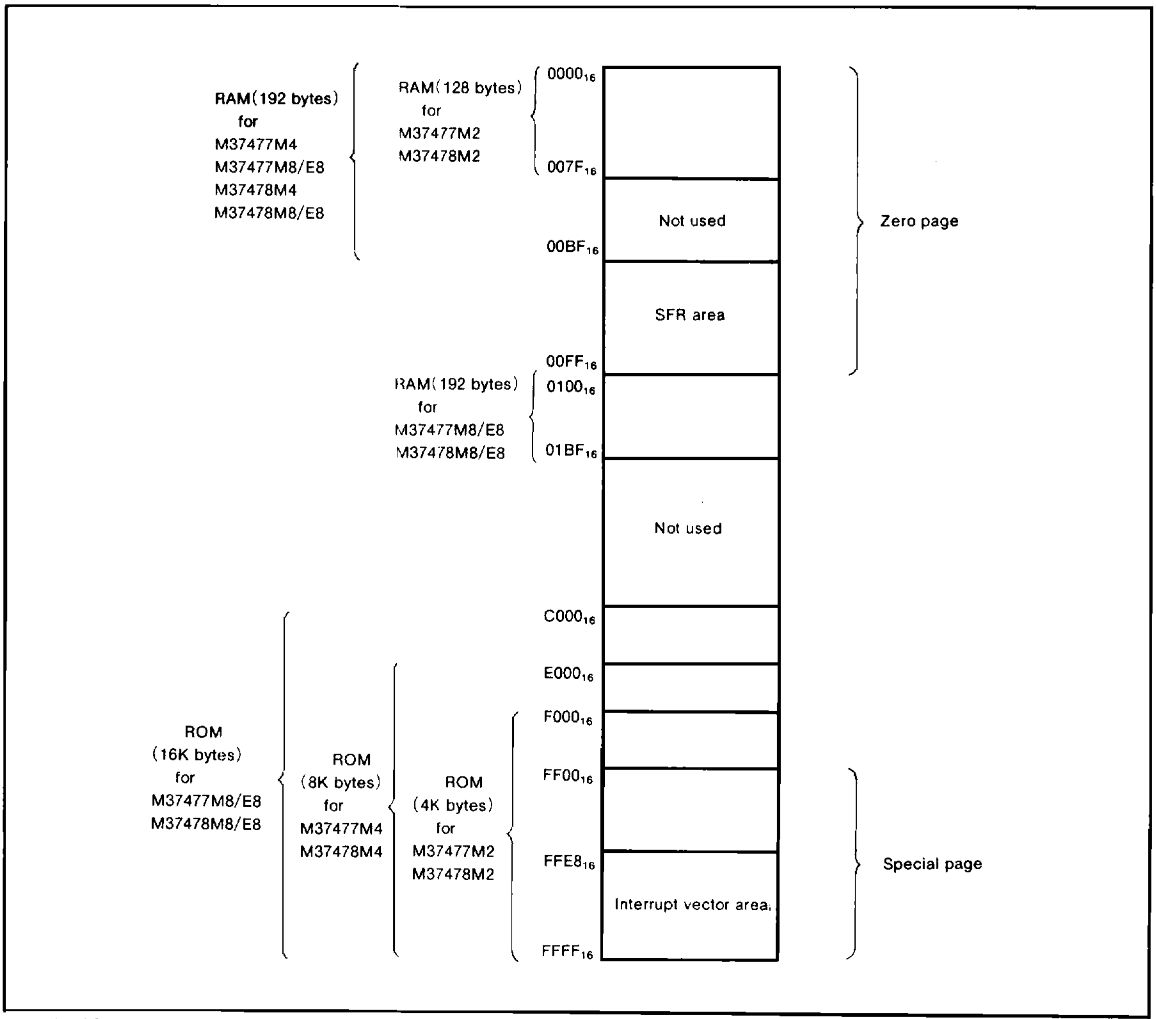


Fig. 2 Memory map

00C0$_{16}$	Port P0
00C1$_{16}$	Port P0 direction register
00C2$_{16}$	Port P1
00C3$_{16}$	Port P1 direction register
00C4$_{16}$	Port P2
00C5$_{16}$	
00C6$_{16}$	Port P3
00C7$_{16}$	
00C8$_{16}$	Port P4
00C9$_{16}$	Port P4 direction register
00CA$_{16}$	Port P5 (Note 1)
00CB$_{16}$	
00CC$_{16}$	
00CD$_{16}$	
00CE$_{16}$	
00CF$_{16}$	
00D0$_{16}$	P0 pull-up control register
00D1$_{16}$	P1−P5 pull-up control register (Note 2)
00D2$_{16}$	
00D3$_{16}$	
00D4$_{16}$	Edge polarity selection register
00D5$_{16}$	
00D6$_{16}$	Input latch register
00D7$_{16}$	
00D8$_{16}$	
00D9$_{16}$	A-D control register
00DA$_{16}$	A-D conversion register
00DB$_{16}$	
00DC$_{16}$	
00DD$_{16}$	
00DE$_{16}$	
00DF$_{16}$	

00E0$_{16}$	Transmit/receive buffer register
00E1$_{16}$	Serial I/O status register
00E2$_{16}$	Serial I/O control register
00E3$_{16}$	UART control register
00E4$_{16}$	Baud rate generator
00E5$_{16}$	
00E6$_{16}$	
00E7$_{16}$	
00E8$_{16}$	
00E9$_{16}$	
00EA$_{16}$	
00EB$_{16}$	
00EC$_{16}$	
00ED$_{16}$	
00EE$_{16}$	
00EF$_{16}$	
00F0$_{16}$	Timer 1
00F1$_{16}$	Timer 2
00F2$_{16}$	Timer 3
00F3$_{16}$	Timer 4
00F4$_{16}$	
00F5$_{16}$	
00F6$_{16}$	
00F7$_{16}$	Timer FF register
00F8$_{16}$	Timer 12 mode register
00F9$_{16}$	Timer 34 mode register
00FA$_{16}$	Timer mode register 2
00FB$_{16}$	CPU mode register
00FC$_{16}$	Interrupt request register 1
00FD$_{16}$	Interrupt request register 2
00FE$_{16}$	Interrupt control register 1
00FF$_{16}$	Interrupt control register 2

Note 1 : This address is not used in the 7477 group.
2 : This address is allocated P1−P4 pull-up control register for the 7477 group.

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 13 different events consisting of five external, seven internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. External interrupts INT_0 and INT_1 can be asserted on either the falling or rising edge as set in the edge polarity selection register. When "0" is set to this register, the interrupt is activated on the falling edge; when "1" is set to the register, the interrupt is activated on the rising edge.

When the device is put into power-down state by the STP instruction or the WIT instruction, if bit 5 in the edge polarity selection register is "1", the INT_1 interrupt becomes a key on wake up interrupt. When a key on wake up interrupt is valid, an interrupt request is generated by applying the "L" level to any pin in port P0. In this case, the port used for interrupt must have been set for the input mode.

If bit 5 in the edge polarity selection register is "0" when the device is in power-down state, the INT_1 interrupt is selected. Also, if bit 5 in the edge polarity selection register is set to "1" when the device is not in a power-down state, neither key on wake up interrupt request nor INT_1 interrupt request is generated.

The $CNTR_0$/$CNTR_1$ interrupts function in the same as INT_0 and INT_1. The interrupt input pin can be specified for either $CNTR_0$ or $CNTR_1$ pin by setting bit 4 in the edge polarity selection register.

Figure 4 shows the structure of the edge polarity selection register, interrupt request registers 1 and 2, and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (polarity programmable)
INT_1 interrupt or key on wake up interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (INT_1 is polarity programmable)
$CNTR_0$ interrupt or $CNTR_1$ interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (polarity programmable)
Timer 1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
Timer 3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 4 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Serial I/O receive interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Serial I/O transmit interrupt	10	$FFED_{16}$, $FFEC_{16}$	
A-D conversion completion interrupt	11	$FFEB_{16}$, $FFEA_{16}$	
BRK instruction interrupt	12	$FFE9_{16}$, $FFE8_{16}$	Non-maskable software interrupt

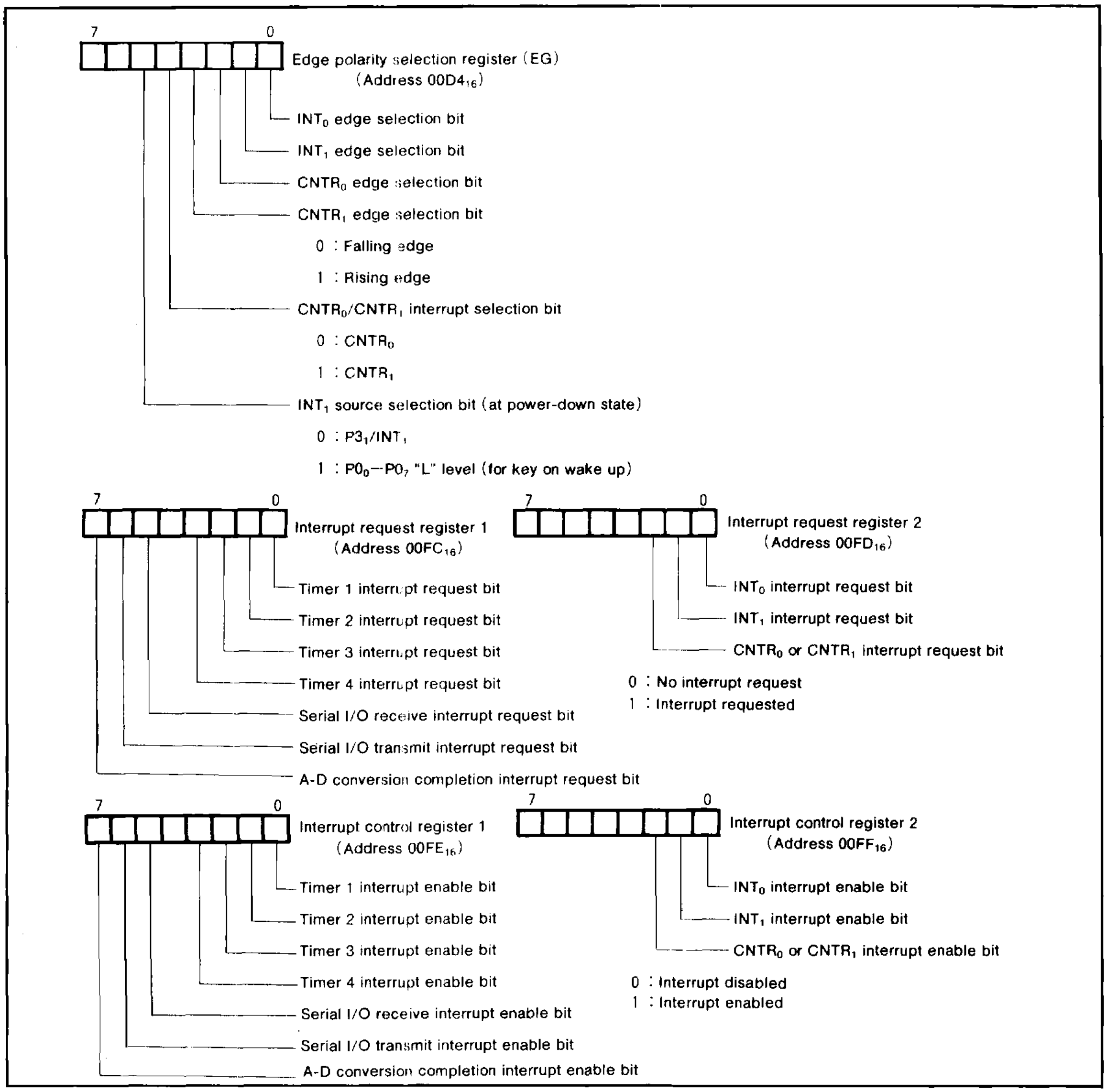


Fig. 4 Structure of registers related to interrupt

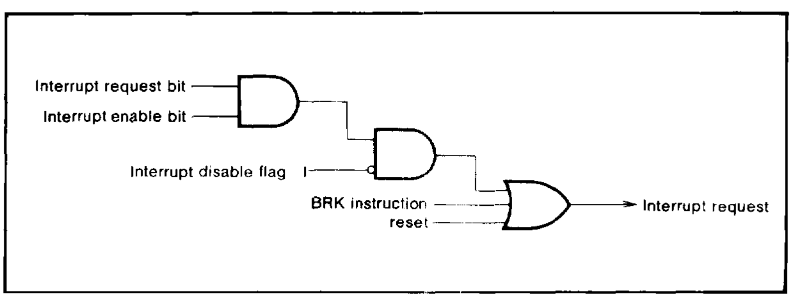


Fig. 5 Interrupt control

TIMER

The 7477/7478 group has four timers; timer 1, timer 2, timer 3, and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

Timer 1 can be operated in the timer mode, event count mode, or pulse output mode. Timer 1 starts counting when bit 0 in the timer 12 mode register (address $00F8_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, or event input from $P3_2/CNTR_0$ pin. Do not select $f(X_{CIN})$ as the count source in the 7477 group. When bit 1 and bit 2 in the timer 12 mode register are "0", $f(X_{IN})$ divided by 16 or $f(X_{CIN})$ divided by 16 is selected. Selection between $f(X_{IN})$ and $f(X_{CIN})$ is done by bit 7 in the CPU mode register (address $00FB_{16}$). When bit 1 in the timer 12 mode register is "0" and bit 2 is "1", $f(X_{CIN})$ is selected. And, when bit 1 in the timer 12 mode register is "1", an event input from the $CNTR_0$ pin is selected. Event inputs are selected depending on bit 2 in the edge polarity selection register (address $00D4_{16}$). When this bit is "0", the inverted value of $CNTR_0$ input is selected; when the bit is "1", $CNTR_0$ input is selected.

When bit 3 in the timer 12 mode register is set to "1", the $P1_2$ pin becomes timer output T_0. When the direction register of $P1_2$ is set for the output mode at this time, the timer 1 overflow divided by 2 is output from T_0.

Please set the initial output value in the following procedure.

① Set "1" to bit 0 of the timer 12 mode register.
  (Timer 1 count stop.)
② Set "1" to bit 0 of the timer mode register 2.
③ Set the output value to bit 0 of the timer FF register.
④ Set the count value to the timer 1.
⑤ Set "0" to bit 0 of the timer 12 mode register.
  (Timer 1 count start.)

Timer 2 can only be operated in the timer mode. Timer 2 starts counting when bit 4 in the timer 12 mode register is set to "0".

The count source can be selected from the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or $f(X_{CIN})$, and timer 1 overflow. Do not select $f(X_{CIN})$ as the count source in the 7477 group. When bit 5 in the timer 12 mode register is "0", any of the divide by 16, divide by 64, divide by 128, or divide by 256 frequency of $f(X_{IN})$ or $f(X_{CIN})$ is selected. The divide ratio is selected according to bit 6 and bit 7 in the timer 12 mode register, and selection between $f(X_{IN})$ and $f(X_{CIN})$ is made according to bit 7 in the CPU mode register. When bit 5 in the timer 12 mode register is "1", timer 1 overflow is selected as the count source.

Timer 3 can be operated in the timer mode, event count mode, or PWM mode. Timer 3 starts counting when bit 0 in the timer 34 mode register (address $00F9_{16}$) is set to "0".

The count source can be selected from the $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pins according to the statuses of bit 1 and bit 2 in the timer 34 mode register, bit 6 in the timer mode register 2 (address $00FA_{16}$) and bit 7 in the CPU mode register. Do not select $f(X_{CIN})$ as the count source in the 7477 group. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 3 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

Timer 4 can be operated in the timer mode, event count mode, pulse output mode, pulse width measuring mode, or PWM mode. Timer 4 starts counting when bit 3 in the timer 34 mode register is set to "0" when bit 6 in this register is "0". When bit 6 is "1", the pulse width measuring mode is selected. The count source can be selected from timer 3 overflow, $f(X_{IN})$ divided by 16, $f(X_{CIN})$ divided by 16, $f(X_{CIN})$, timer 1 or timer 2 overflow, or an event input from $P3_3/CNTR_1$ pin according to the statuses of bit 4 and bit 5 in the timer 34 mode register, bit 6 in the timer mode register 2, and bit 7 in the CPU mode register. Do not select $f(X_{CIN})$ as the count source in the 7477 group. Note, however, that if timer 1 overflow or timer 2 overflow is selected for the count source of timer 4 when timer 1 overflow is selected for the count source of timer 2, timer 1 overflow is always selected regardless of the status of bit 6 in the timer mode register 2. Event inputs are selected depending on bit 3 in the edge polarity selection register. When this bit is "0", the inverted value of $CNTR_1$ input is selected; when the bit is "1", $CNTR_1$ input is selected.

When bit 7 in the timer 34 mode register is set to "1", the $P1_3$ pin becomes timer output T_1. When the direction register of $P1_3$ is set for the output mode at this time, the timer 4 overflow divided by 2 is output from T_1 when bit 7 in the timer mode register 2 is "0".

Please set the initial output value in the following procedure.

① Set "1" to bit 3 of the timer 34 mode register.
  (Timer 4 count stop.)
② Set "1" to bit 1 of the timer mode register 2.
③ Set the output value to bit 1 of the timer FF register.
④ Set the count value to the timer 4.
⑤ Set "0" to bit 3 of the timer 34 mode register.
  (Timer 4 count start.)

(1) Timer mode

Timer performs down count operations with the dividing ratio being $1/(n+1)$. Writing a value to the timer latch sets a value to the timer. When the value to be set to the timer latch is nn_{16}, the value to be set to a timer is nn_{16}, which is down counted at the falling edge of the count source from nn_{16} to (nn_{16}-1) to (nn_{16}-2) to...01_{16} to 00_{16} to FF_{16}. At the falling edge of the count source immediately after timer value has reached FF_{16}, value (nn_{16}-1) obtained by subtracting one from the timer latch value is set (reloaded) to the timer to continue counting. At the rising edge of the count source immediately after the timer value has reached FF_{16}, an overflow occurs and an interrupt request is generated.

(2) Event count mode

Timer operates in the same way as in the timer mode except that it counts input from the $CNTR_0$ or $CNTR_1$ pin.

(3) Pulse output mode

In this mode, duty 50% pulses are output from the T_0 or T_1 pin. When the timer overflows, the polarity of the T_0 or T_1 pin output level is inverted.

(4) Pulse width measuring mode

The 7477/7478 group can measure the "H" or "L" width of the $CNTR_0$ or $CNTR_1$ input waveform by using the pulse width measuring mode of timer 4. The pulse width measuring mode is selected by writing "1" to bit 6 in the timer 34 mode register. In the pulse width measuring mode, the timer counts the count source while the $CNTR_0$ or $CNTR_1$ input is "H" or "L". Whether the $CNTR_0$ input or $CNTR_1$ input to be measured can be specified by the status of bit 4 in the edge polarity selection register; whether the "H" width or "L" width to be measured can be specified by the status of bit 2 ($CNTR_0$) and bit 3 ($CNTR_1$) in the edge polarity selection register.

(5) PWM mode

The PWM mode can be entered for timer 3 and timer 4 by setting bit 7 in the timer mode register 2 to "1". In the PWM mode, the $P1_3$ pin is set for timer output T_1 to output PWM waveforms by setting bit 7 in the timer 34 mode register to "1". The direction register of $P1_3$ must be set for the output mode before this can be done.

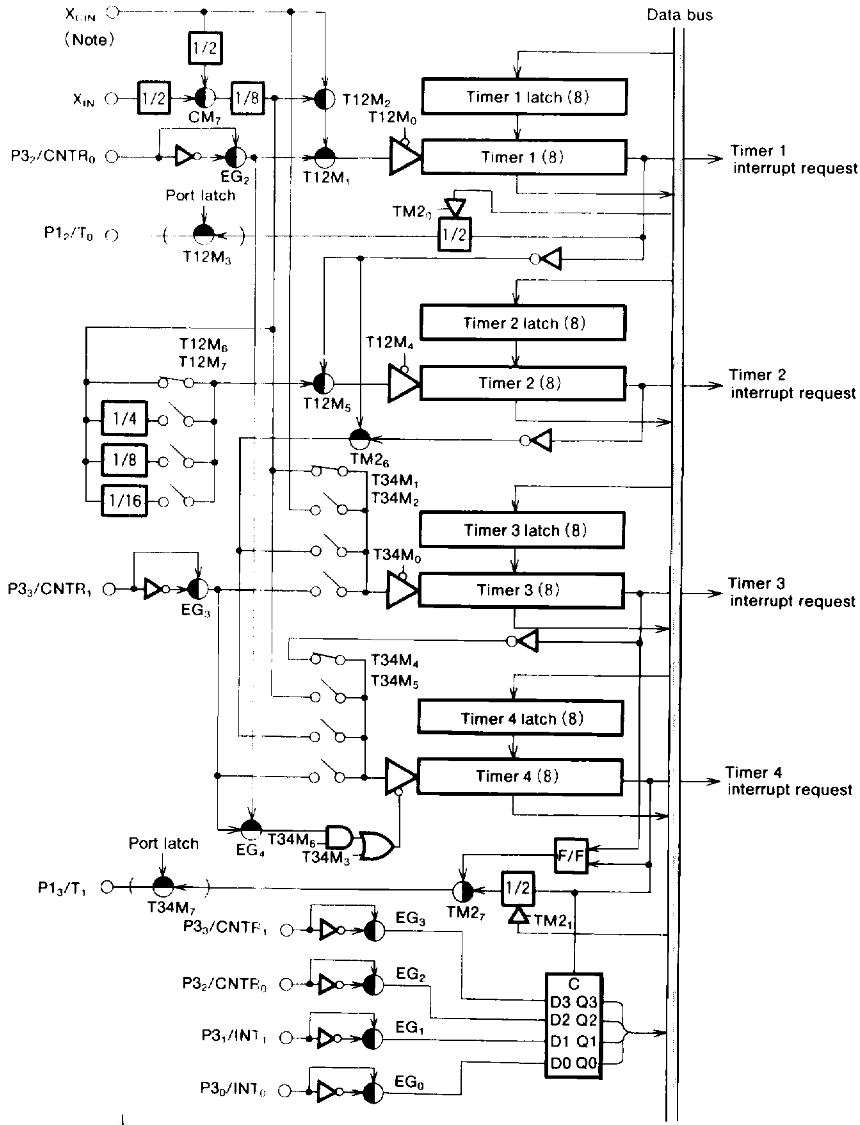
In the PWM mode, timer 3 is counting and timer 4 is idle while the PWM waveform is "L". When timer 3 overflows, the PWM waveform goes "H". At this time, timer 3 stops counting simultaneously and timer 4 starts counting. When timer 4 overflows, the PWM waveform goes "L", and timer 4 stops and timer 3 starts counting again. Consequently, the "L" duration of the PWM waveform is determined by the value of timer 3; the "H" duration of the PWM waveform is determined by the value of timer 4.

When a value is written to the timer in operation during the PWM mode, the value is only written to the timer latch, and not written to the timer. In this case, if the timer overflows, a value one less the value in the timer latch is written to the timer. When any value is written to an idle timer, the value is written to both the timer latch and the timer.

In this mode, do not select timer 3 overflow as the count source for timer 4.

INPUT LATCH FUNCTION

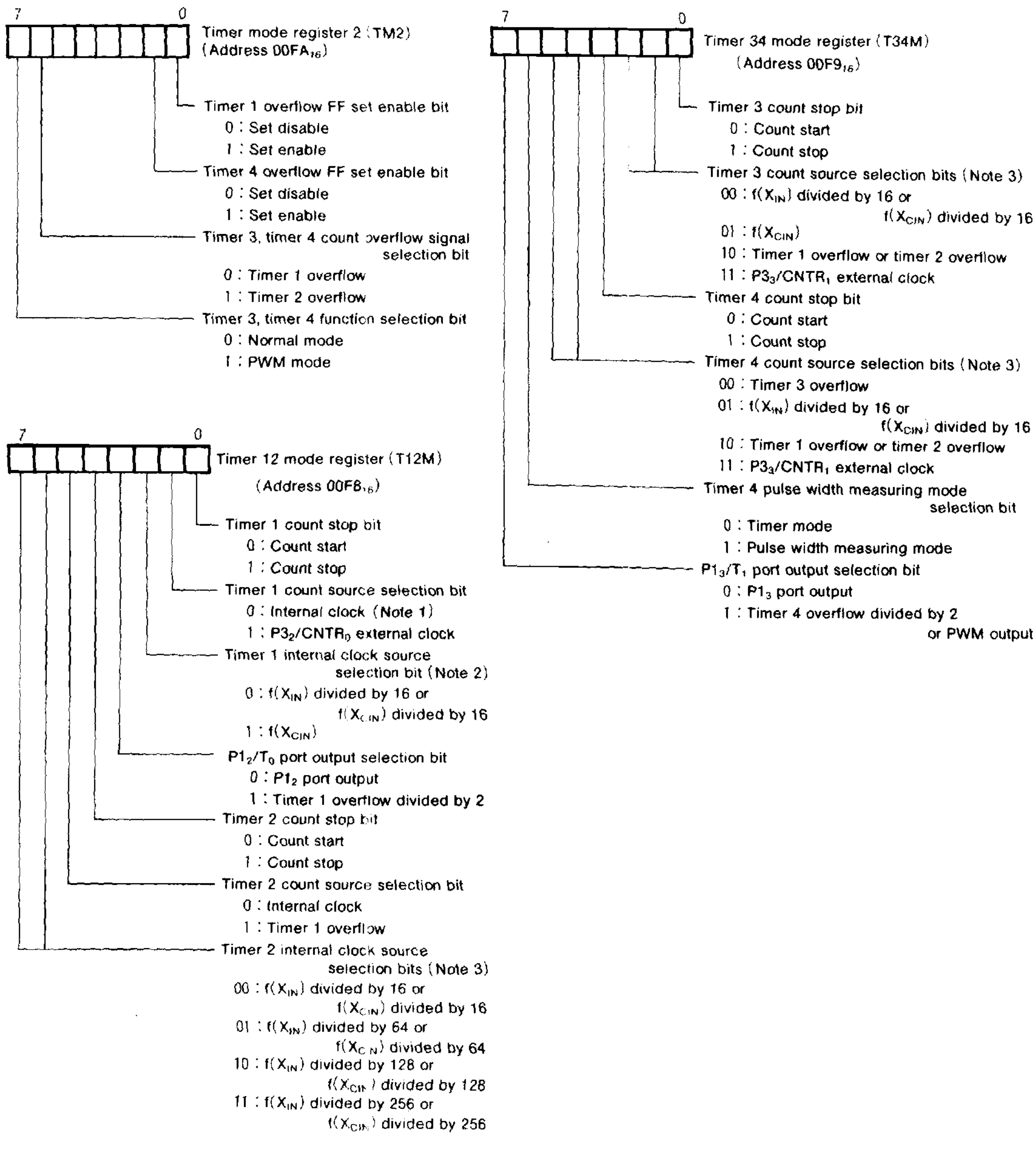
The 7477/7478 group can latch the $P3_0/INT_0$, $P3_1/INT_1$, $P3_2/CNTR_0$, and $P3_3/CNTR_1$ pin level into the input latch register (address $00D6_{16}$) when timer 4 overflows. The polarity of each pin latched to the input latch register can be selected by using the edge polarity selection register. When bit 0 in the edge polarity selection register is "0", the inverted value of the $P3_0/INT_0$ pin level is latched; when the bit is "1", the $P3_0/INT_0$ pin level is latched as it is. When bit 1 in the edge polarity selection register is "0", the inverted value of the $P3_1/INT_1$ pin level is latched; when the bit is "1", the $P3_1/INT_1$ pin level is latched as it is. When bit 2 in the edge polarity selection register is "0", the inverted value of the $P3_2/CNTR_0$ pin level is latched; when the bit is "1", the $P3_2/CNTR_0$ pin level is latched as it is. When bit 3 in the edge polarity selection register is "0", the inverted value of the $P3_3/CNTR_1$ pin level is latched; when the bit is "1", the $P3_3/CNTR_1$ pin level is latched as it is.



(Select gate : At reset, shaded side is connected.)

Note : The 7477 group does not have X_{CIN} input.

Fig. 6 Block diagram of timer 1 through 4



Note 1 : $f(X_{IN})$ divided by 16 in the 7477 group.
2 : The 7477 group does not use this bit (bit 2). Set this bit to "0".
3 : Do not select $f(X_{CIN})$ as the count source in the 7477 group.

Fig. 7 Structure of timer mode registers

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O control register to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

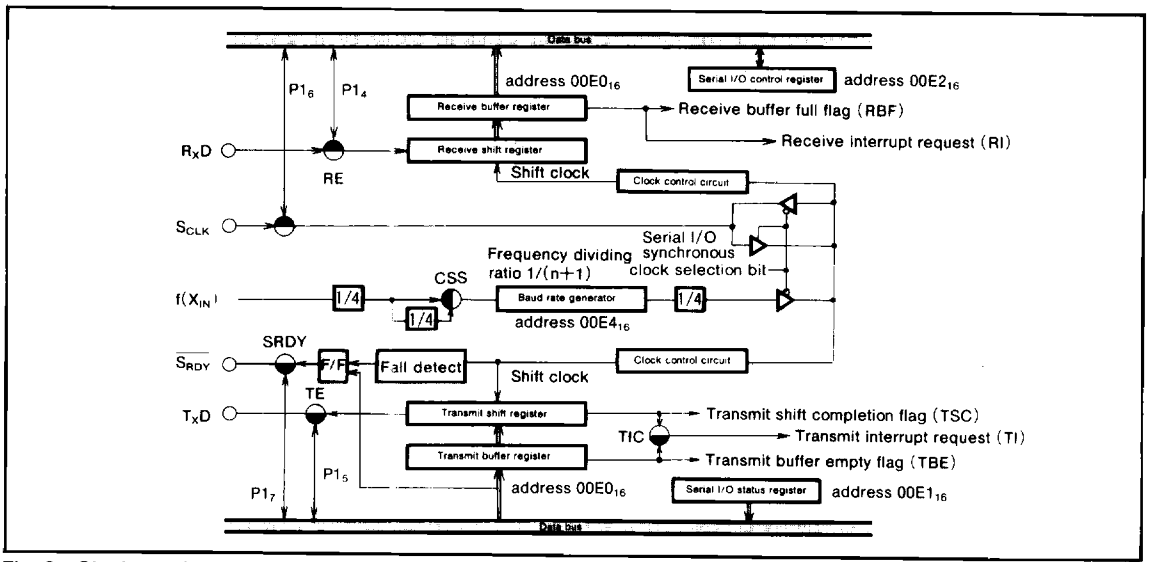
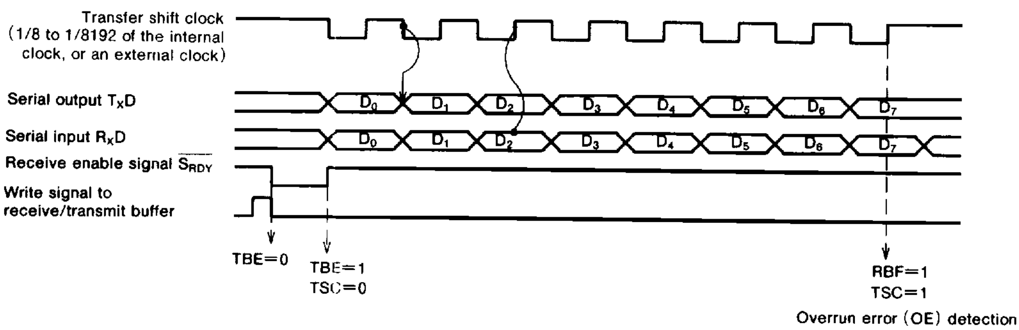


Fig. 8 Clock synchronous serial I/O block diagram



Note 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.

2 : If data is written to the transmit buffer when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the T_XD pin.

3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 9 Operation of clock synchronous serial I/O function

Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical. The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

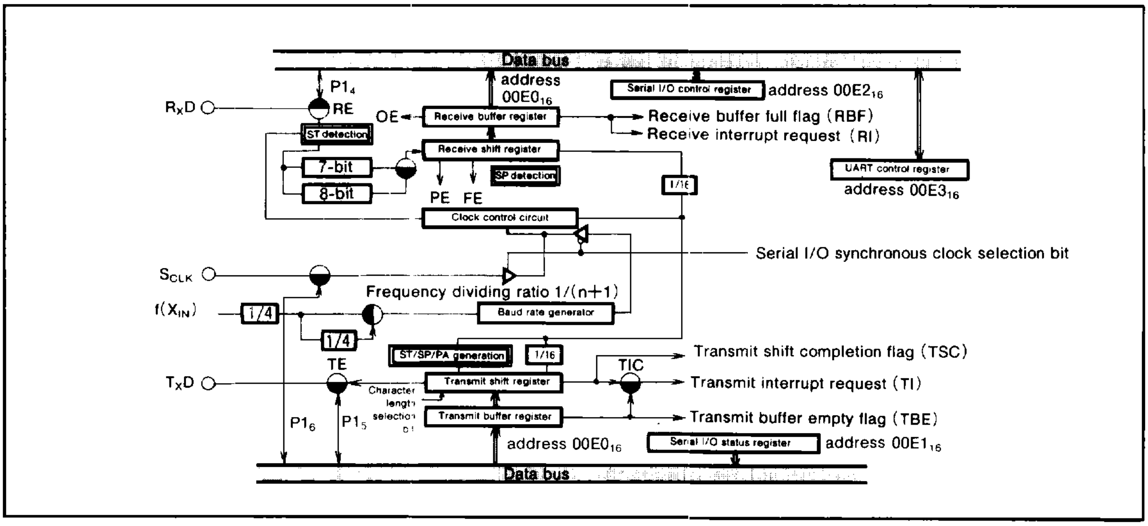
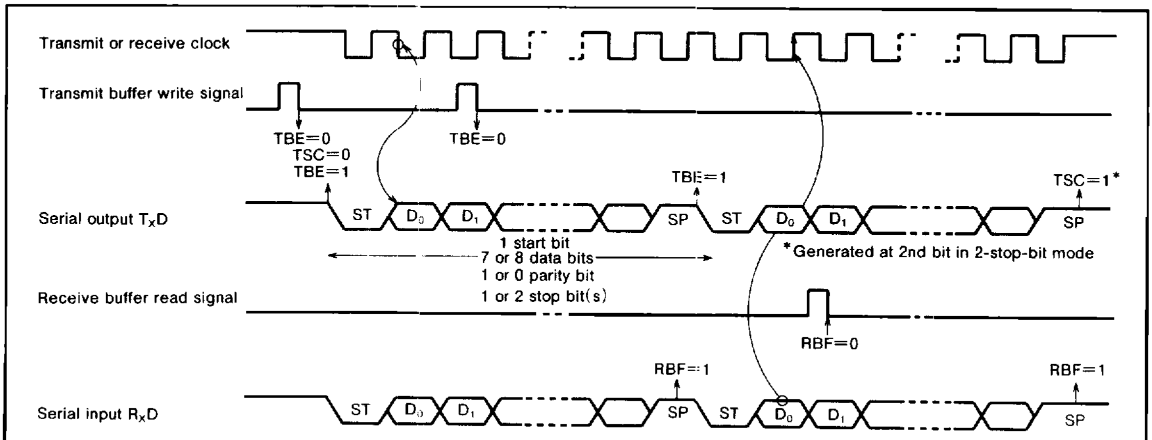


Fig. 10 UART serial I/O block diagram



Note 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".

Fig. 11 Operation of UART serial I/O function

Serial I/O Control Register SIOCON

The serial I/O control register consists of eight control bits for the serial I/O function.

UART Control Register UARTCON

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer.

Serial I/O Status Register SIOSTS

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. Writing to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

Transmit Buffer/Receive Buffer TB/RB

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

Baud Rate Generator BRG

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the baud rate generator.

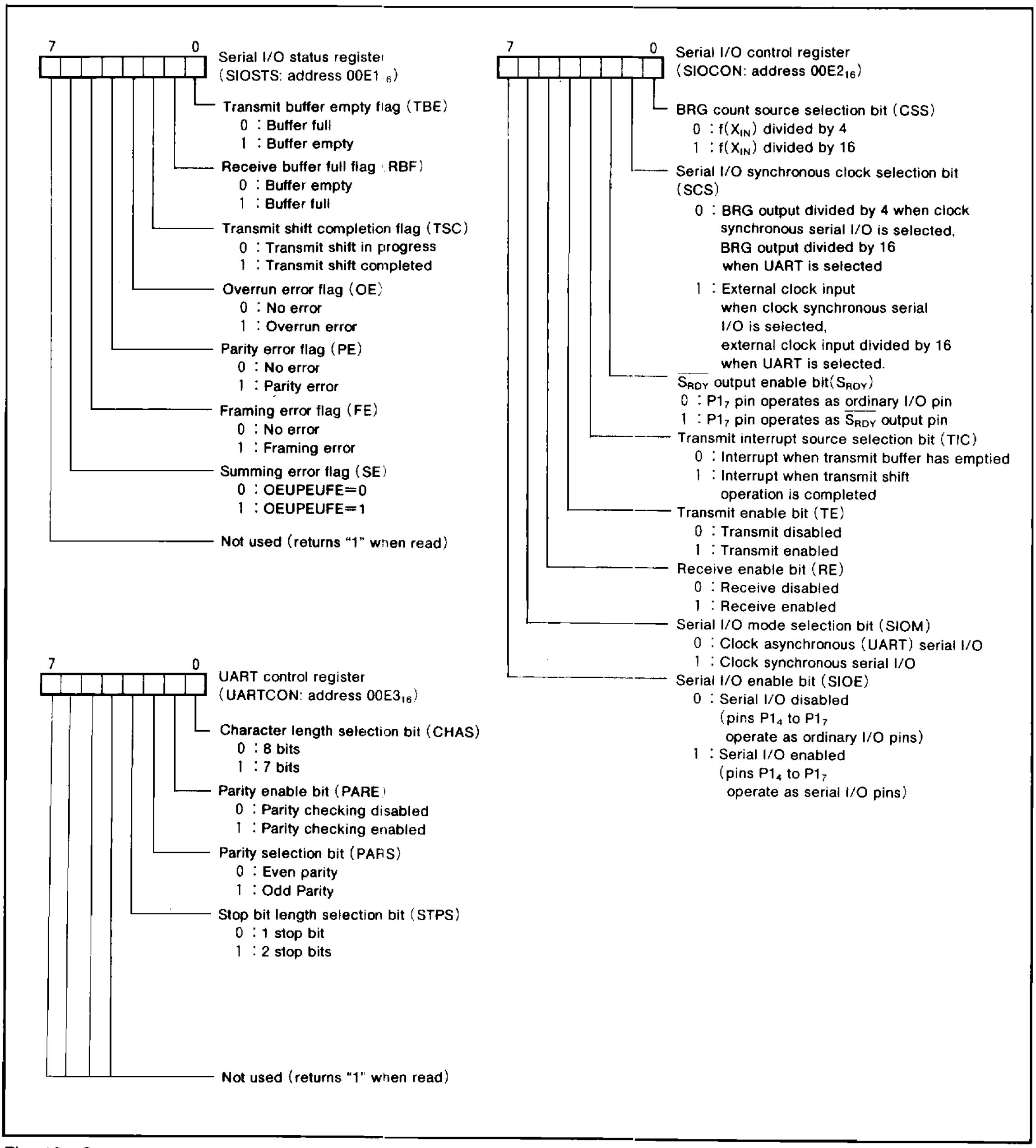


Fig. 12 Structure of serial I/O control registers

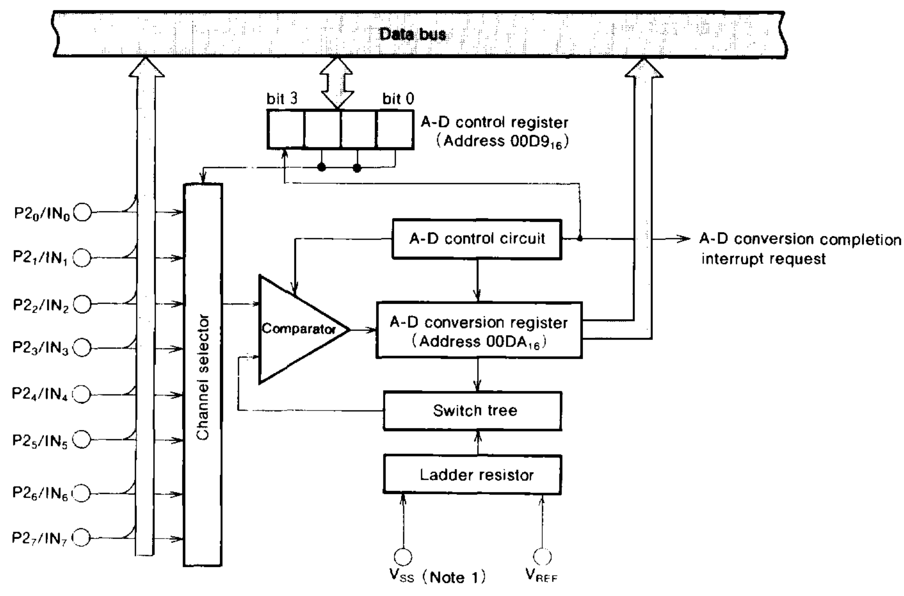
A-D CONVERTER

The A-D conversion uses an 8-bit successive comparison method. Figure 13 shows a block diagram of the A-D conversion circuit. Conversion is automatically carried out once started by the program.

There are eight analog input pins which are shared with $P2_0$ to $P2_7$ of port P2 (Only $P2_0$ to $P2_3$ 4-bit for 7477 group). Which analog inputs are to be A-D converted is specified by using bit 2 to bit 0 in the A-D control register (address $00D9_{16}$). Pins for inputs to be A-D converted must be set for input by setting the direction register bit to "0". Bit 3 in the A-D control register is an A-D conversion end bit. This is "0" during A-D conversion; it is set to "1" when the conversion is terminated. Therefore, it is possible to know whether A-D conversion is terminated by checking this bit. Figure 14 shows the relationship between the contents of A-D control register and the selected input pins.

The A-D conversion register (address $00DA_{16}$) contains information on the results of conversion, so that it is possible to know the results of conversion by reading the contents of this register.

The following explains the procedure to execute A-D conversion. First, set values to bit 2 to bit 0 in the A-D control register to select the pins that you want to execute A-D conversion. Next, clear the A-D conversion end bit to "0". When the above is done, A-D conversion is initiated. The A-D conversion is completed after an elapse of 50 machine cycles (12.5μs when $f(X_{IN})=8MHz$), the A-D conversion end bit is set to "1", and the interrupt request bit is set to "1". The results of conversion are contained in the A-D conversion register.



Note 1 : AV_{SS} for M37478M2/M4/M8/E8-XXXFP
2 : The 7477 group does not have $P2_4/IN_4$ to $P2_7/IN_7$.

Fig. 13 A-D converter circuit

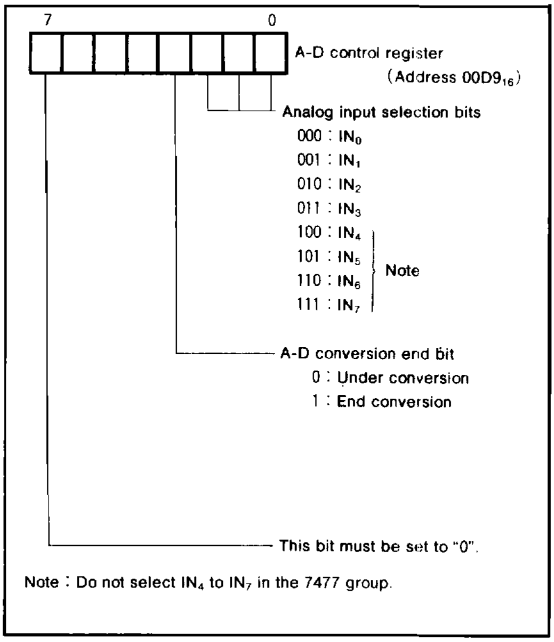


Fig. 14 Structure of A-D control register

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P0 has "L" level applied, after bit 5 of the edge polarity selection register (EG_5) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. A key matrix can be connected to port P0 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_1}$ interrupt. When EG_5 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_1}$ are invalid.

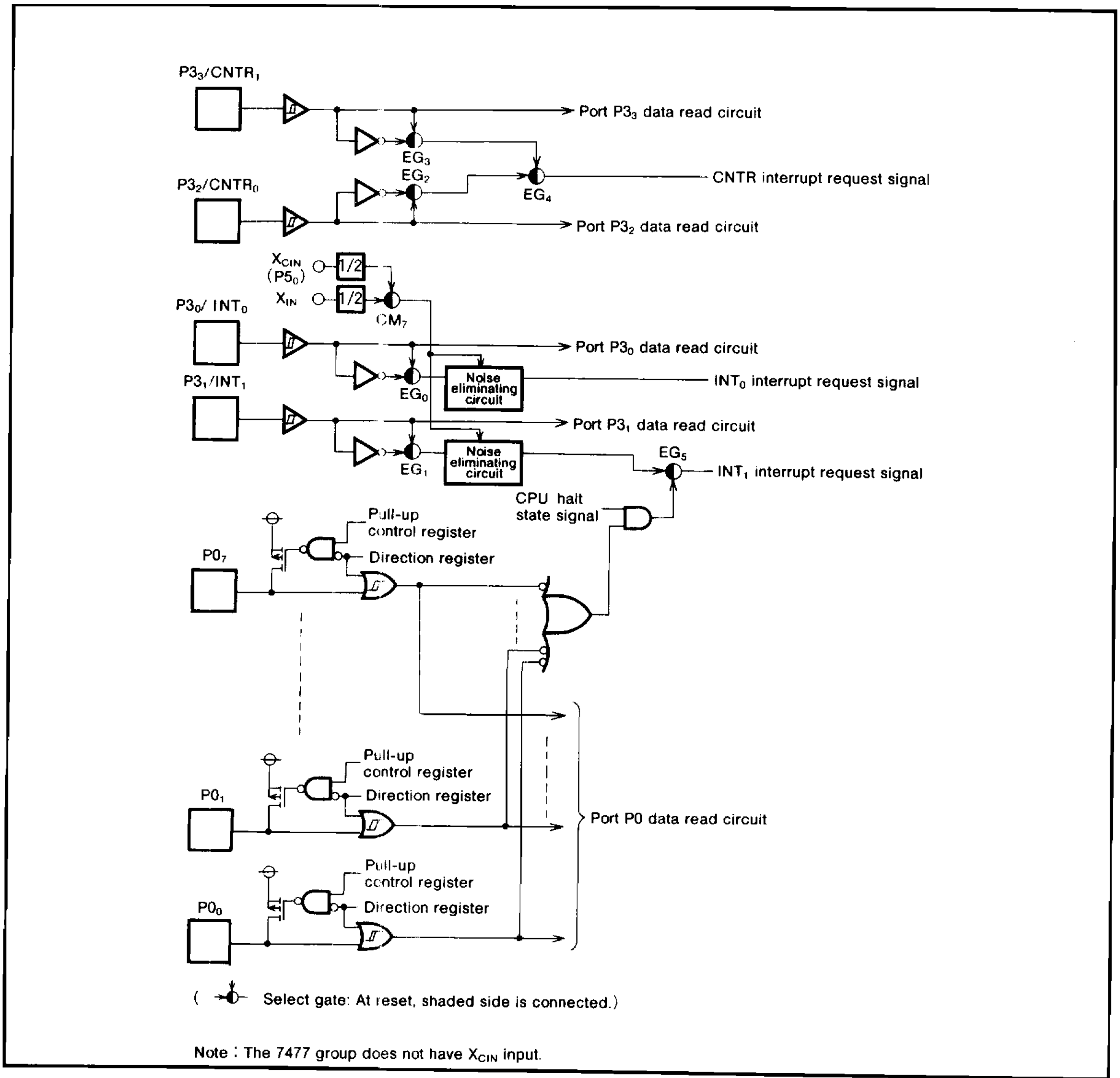


Fig. 15 Block diagram of interrupt input and key on wake up circuit

RESET CIRCUIT

The 7477/7478 group is reset according to the sequence shown in Figure 18. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is in the recommended operating condition and then returned to "H" level.

The internal initializations following reset are shown in Figure 17.

Example of reset circuit is Figure 16. Immediately after reset, timer 3 and timer 4 are connected, and counts the $f(X_{IN})$ divided by 16. At this time, FF_{16} is set to timer 3, and 07_{16} is set to timer 4. The reset is cleared when timer 4 overflows.

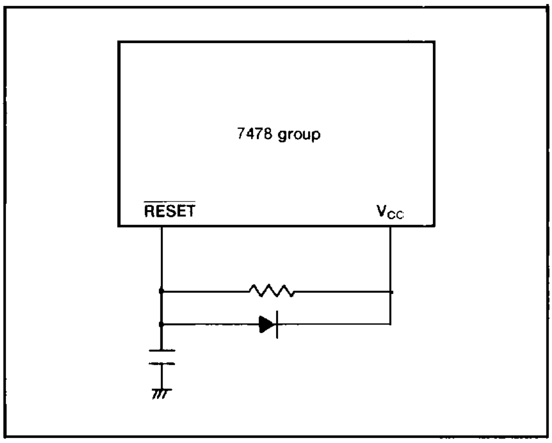


Fig. 16 Example of reset circuit

No.	Register	Address								
(1)	Port P0 direction register	$(C1_{16})$···	00_{16}							
(2)	Port P1 direction register	$(C3_{16})$···	00_{16}							
(3)	Port P4 direction register	$(C9_{16})$···					0	0	0	0
(4)	P0 pull-up control register	$(D0_{16})$···	00_{16}							
(5)	P1−P5 pull-up control register (Note 1)	$(D1_{16})$···		0		0			0	0
(6)	Edge selection register (EG)	$(D4_{16})$···			0	0	0	0	0	0
(7)	A-D control register	$(D9_{16})$···	0				1	0	0	0
(8)	Serial I/O status register	$(E1_{16})$···		0	0	0	0	0	0	0
(9)	Serial I/O control register	$(E2_{16})$···	00_{16}							
(10)	UART control register	$(E3_{16})$···					0	0	0	0
(11)	Timer 12 mode register (T12M)	$(F8_{16})$···	00_{16}							
(12)	Timer 34 mode register (T34M)	$(F9_{16})$···	00_{16}							
(13)	Timer mode register 2 (TM2)	(FA_{16})···	0	0					0	0
(14)	CPU mode register (CM)	(FB_{16})···	0	0	0	0		0	0	0
(15)	Interrupt request register 1	(FC_{16})···	0	0			0	0	0	0
(16)	Interrupt request register 2	(FD_{16})···						0	0	0
(17)	Interrupt control register 1	(FE_{16})···	0	0			0	0	0	0
(18)	Interrupt control register 2	(FF_{16})···						0	0	0
(19)	Program counter	(PC_H)···	Contents of address $FFFF_{16}$							
		(PC_L)···	Contents of address $FFFE_{16}$							
(20)	Processor status register	(PS)···						1		

Note 1 : This address is allocated P1−P4 pull-up control register for the 7477 group. Bit 6 is not used.
2 : Since the contents of both registers other than those listed above (including timers and the transmit/receive buffer register) are undefined at reset, it is necessary to set initial values.

Fig. 17 Internal state of microcomputer at reset

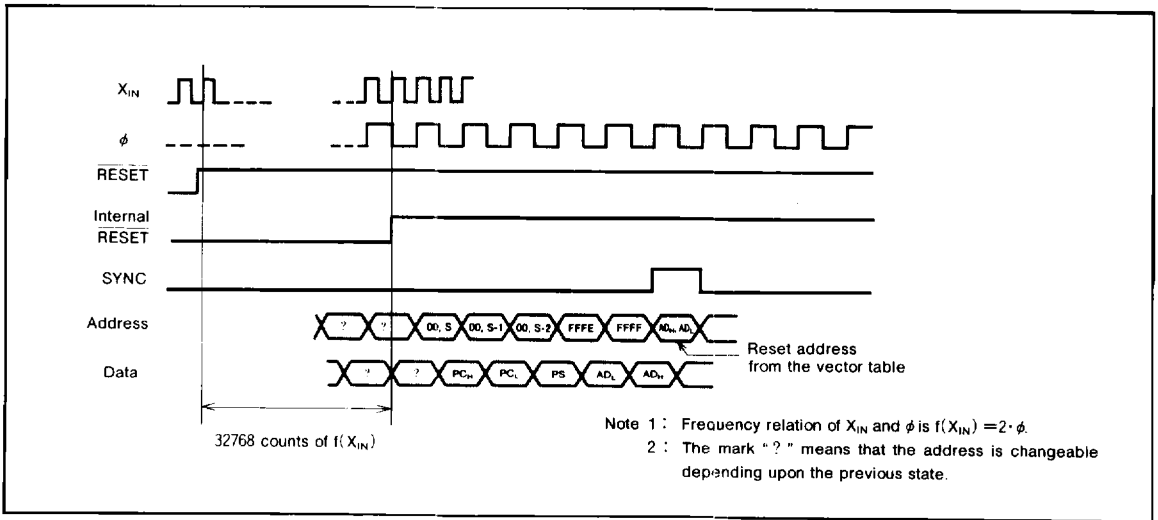


Fig. 18 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs. As shown in Figure 2, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's direction register allows each bit to be programmed individually as input or output. The direction register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port latch and output. When data is read from the output port, the output pin level is not read, only the latched data of the port latch is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output latch and the pin still remains in the high impedance state. Following the execution of STP or WIT instruction, key matrix with port P0 can be used to generate the interrupt to bring the microcomputer back in its normal state. When this port is selected for input, pull-up transistor can be connected in units of 1-bit.

(2) Port P1

Port P1 has the same function as port P0. $P1_2-P1_7$ serve dual functions, and the desired function can be selected by the program. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(3) Port P2

Port P2 is an 8-bit input port. In the 7477 group, this port is $P2_0-P2_3$, a 4-bit input port. This port can also be used as the analog voltage input pins.

(4) Port P3

Port P3 is a 4-bit input port.

(5) Port P4

Port P4 is a 4-bit I/O port and has basically the same functions as port P0. In the 7477 group, this port is $P4_0$ and $P4_1$, a 2-bit I/O port. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.

(6) Port P5

Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$ and $P5_1$ are shared with clock generating circuit input/output pins.

The 7477 group does not have this port.

(7) INT_0 pin ($P3_0/INT_0$ pin)

This is an interrupt input pin, and is shared with port $P3_0$. When "H" to "L" or "L" to "H" transition input is applied to this pin, the INT_0 interrupt request bit (bit 0 of address $00FD_{16}$) is set to "1".

(8) INT_1 pin ($P3_1/INT_1$ pin)

This is an interrupt input pin, and is shared with port $P3_1$. When "H" to "L" or "L" to "H" transition input is applied to this pin, the INT_1 interrupt request bit (bit 1 of address $00FD_{16}$) is set to "1".

(9) Counter input $CNTR_0$ pin ($P3_2/CNTR_0$ pin)

This is a timer input pin, and is shared with port $P3_2$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and "H" to "L" or "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

(10) Counter input $CNTR_1$ pin ($P3_3/CNTR_1$ pin)

This is a timer input pin, and is shared with port $P3_3$. When this pin is selected to $CNTR_0$ or $CNTR_1$ interrupt input pin and "H" to "L" or "L" to "H" transition input is applied to this pin, the $CNTR_0$ or $CNTR_1$ interrupt request bit (bit 2 of address $00FD_{16}$) is set to "1".

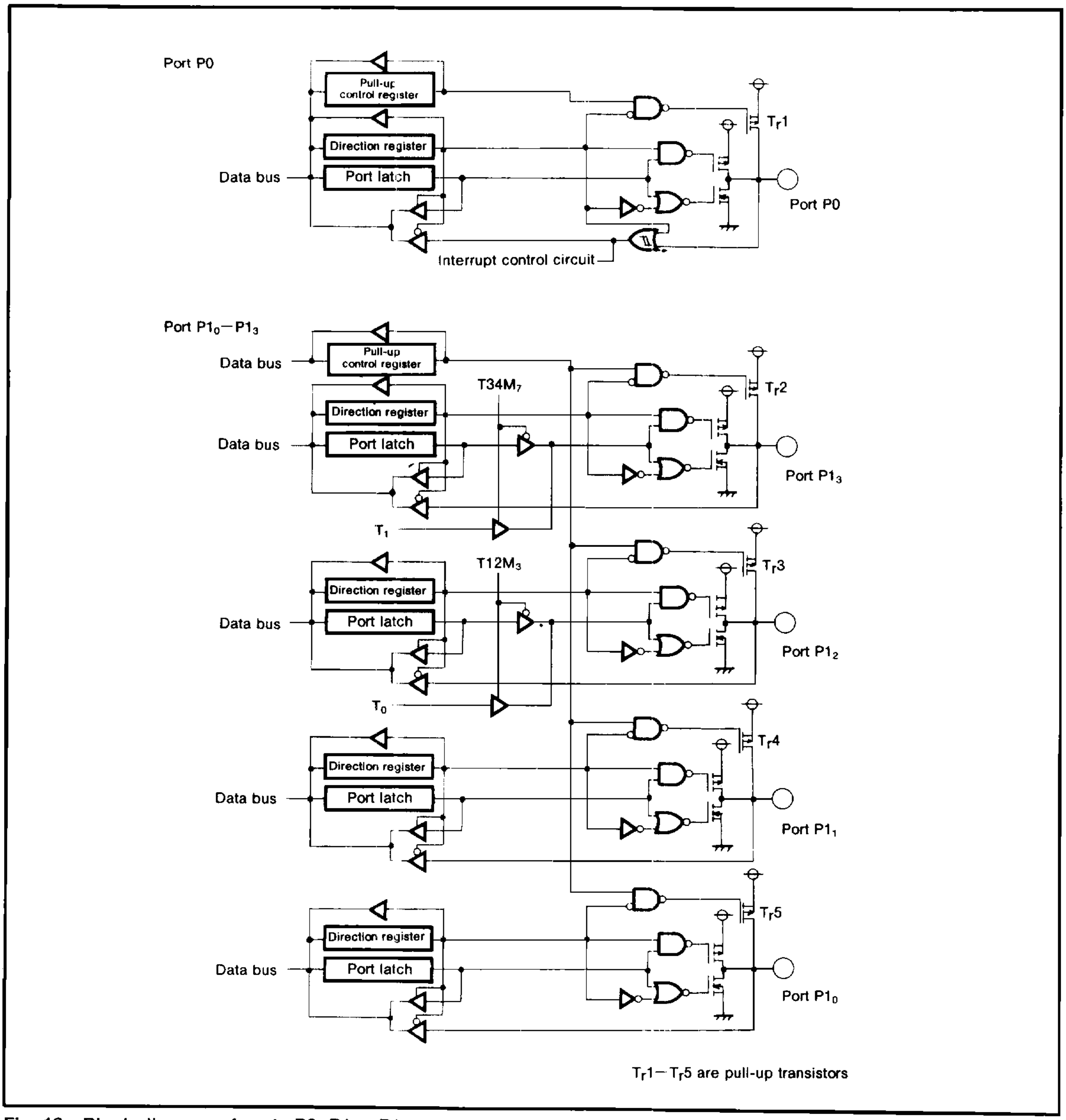


Fig. 19 Block diagram of ports P0, $P1_0-P1_3$

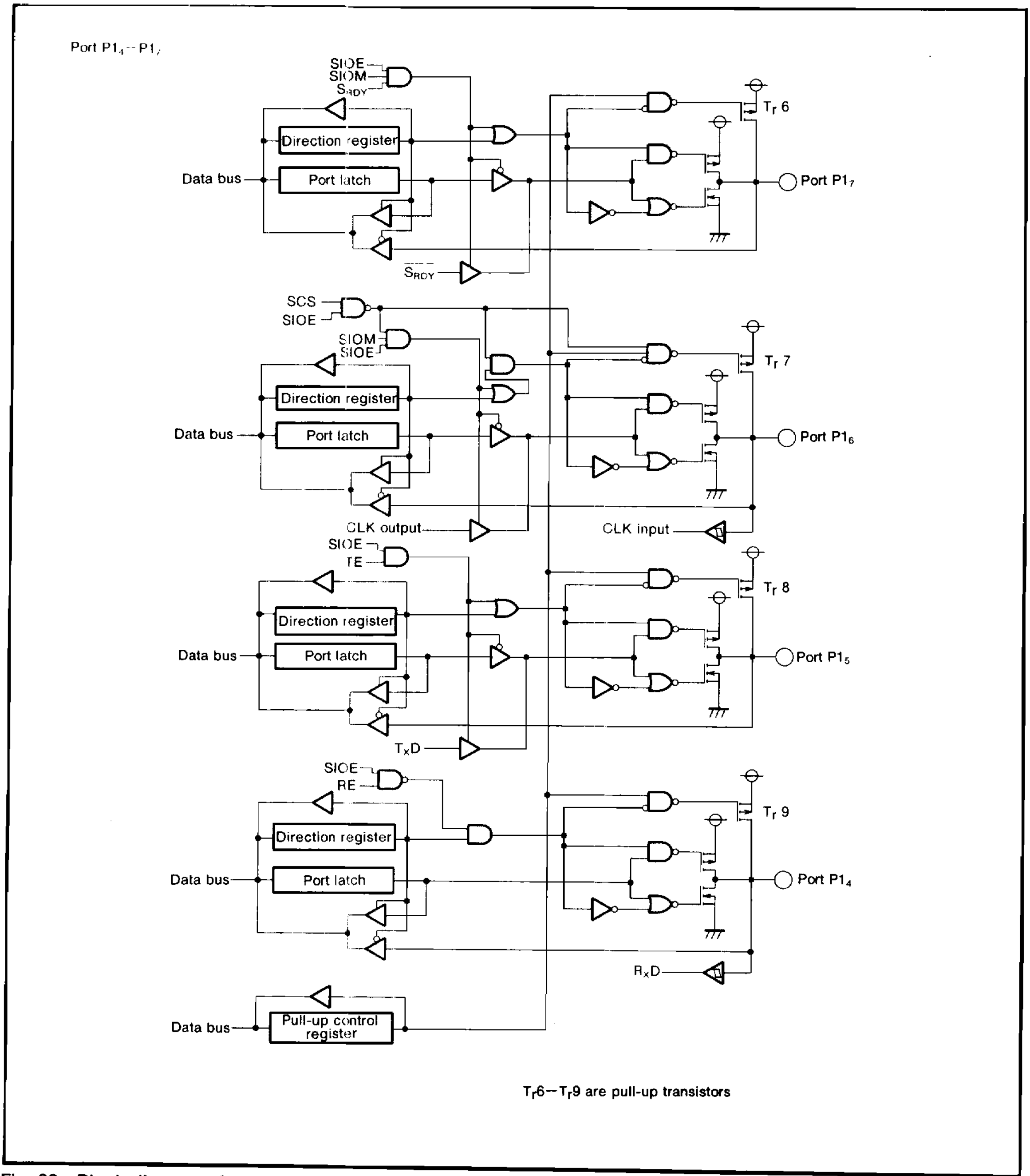


Fig. 20 Block diagram of ports $P1_4$–$P1_7$

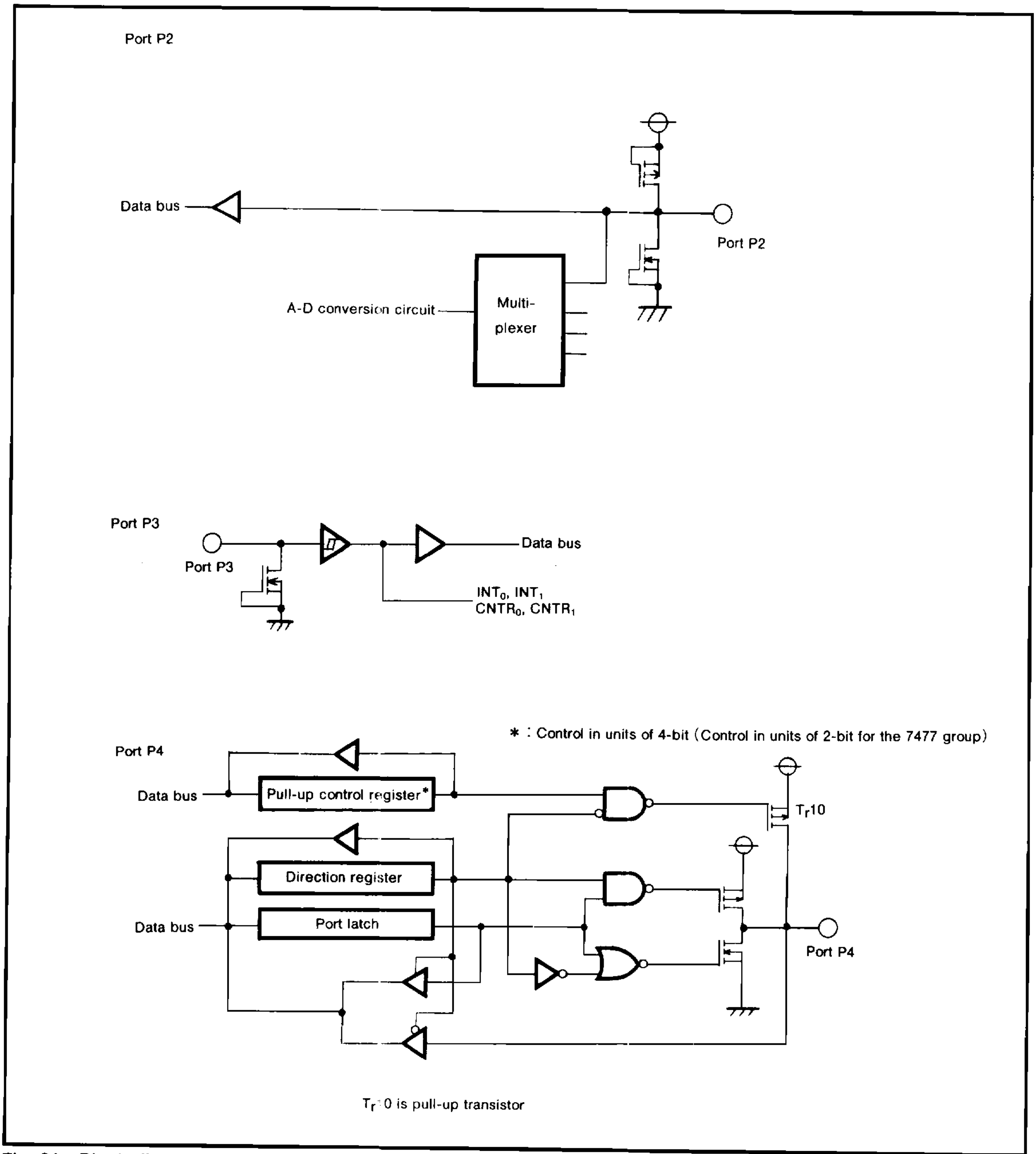


Fig. 21 Block diagram of ports P2—P4

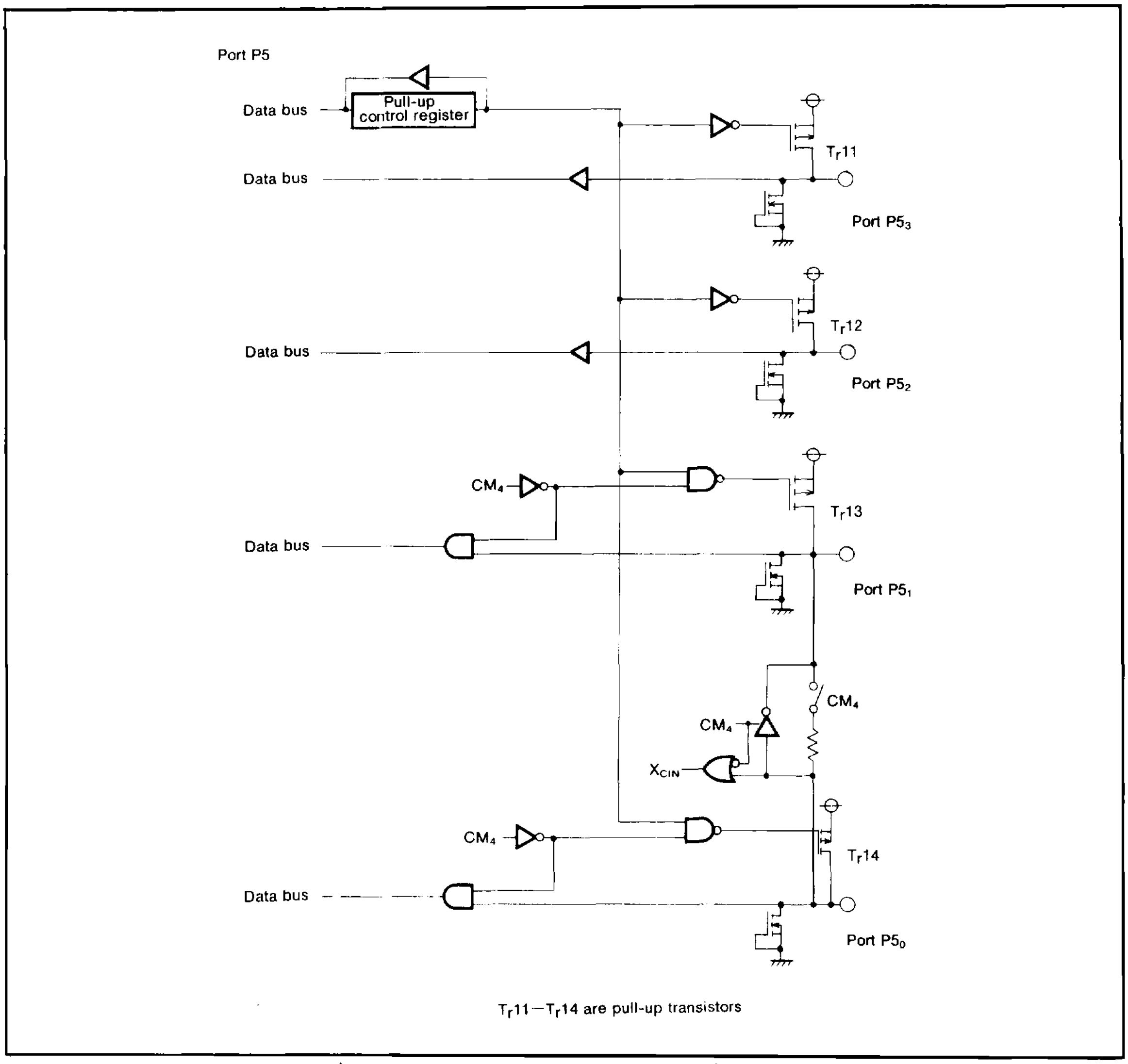


Fig. 22 Block diagram of port P5 (The 7477 group does not have this port)

CLOCK GENERATING CIRCUIT

The 7477 group has one internal clock generating circuit and 7478 group has two internal clock generating circuits. Figure 27 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by two is used as the internal clock ϕ. Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN} in the 7478 group.

Figure 23, 24 show a circuit example using a ceramic resonator (or quartz crystal oscillator). Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN}(X_{CIN}) pin and leave the X_{OUT}(X_{COUT}) pin open. A circuit example is shown in Figure 25, 26.

The 7477/7478 group has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and FF_{16} is automatically set in timer 3 and 07_{16} in timer 4.

Although oscillation is restarted when an external interrupt is accepted, the internal clock ϕ remains in the "H" state until timer 4 overflows. In other words, the internal clock ϕ is not supplied until timer 4 overflows. This is because when a ceramic or similar other oscillator is used, a finite time is required until stable oscillation is obtained after restart.

The microcomputer enters an wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode or the stop mode must be set to "1" before executing the WIT or the STP instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (30μA typ. at $f(X_{CIN})=32$kHz) This operation is only 7478 group. X_{IN} clock oscillation is stopped when the bit 6 of CPU mode register is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 29 shows the transition of states for the system clock.

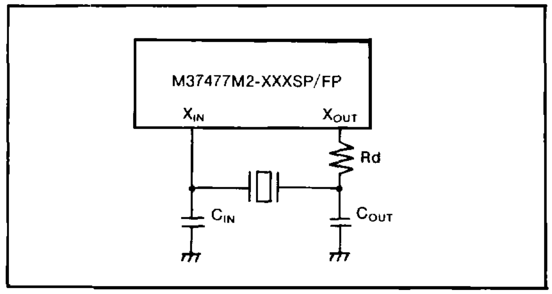


Fig. 23 Example of ceramic resonator circuit (M37477)

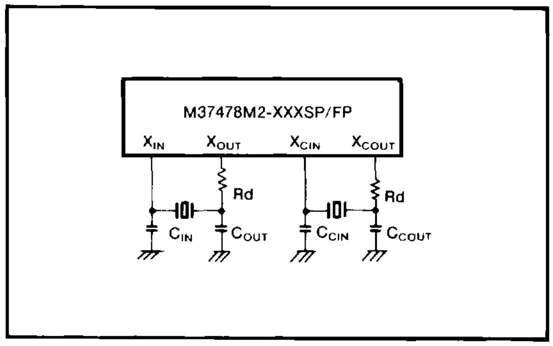


Fig. 24 Example of ceramic resonator circuit (M37478)

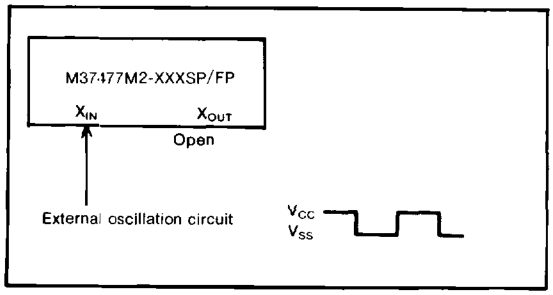


Fig. 25 External clock input circuit (M37477)

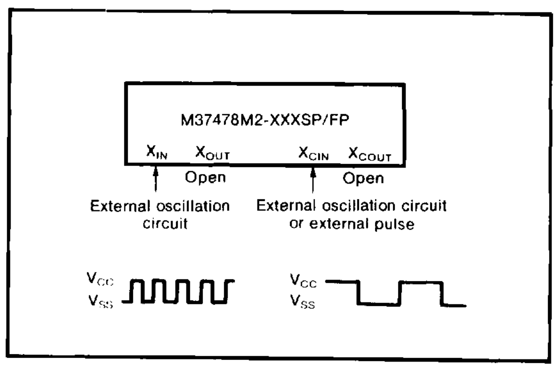


Fig. 26 External clock input circuit (M37478)

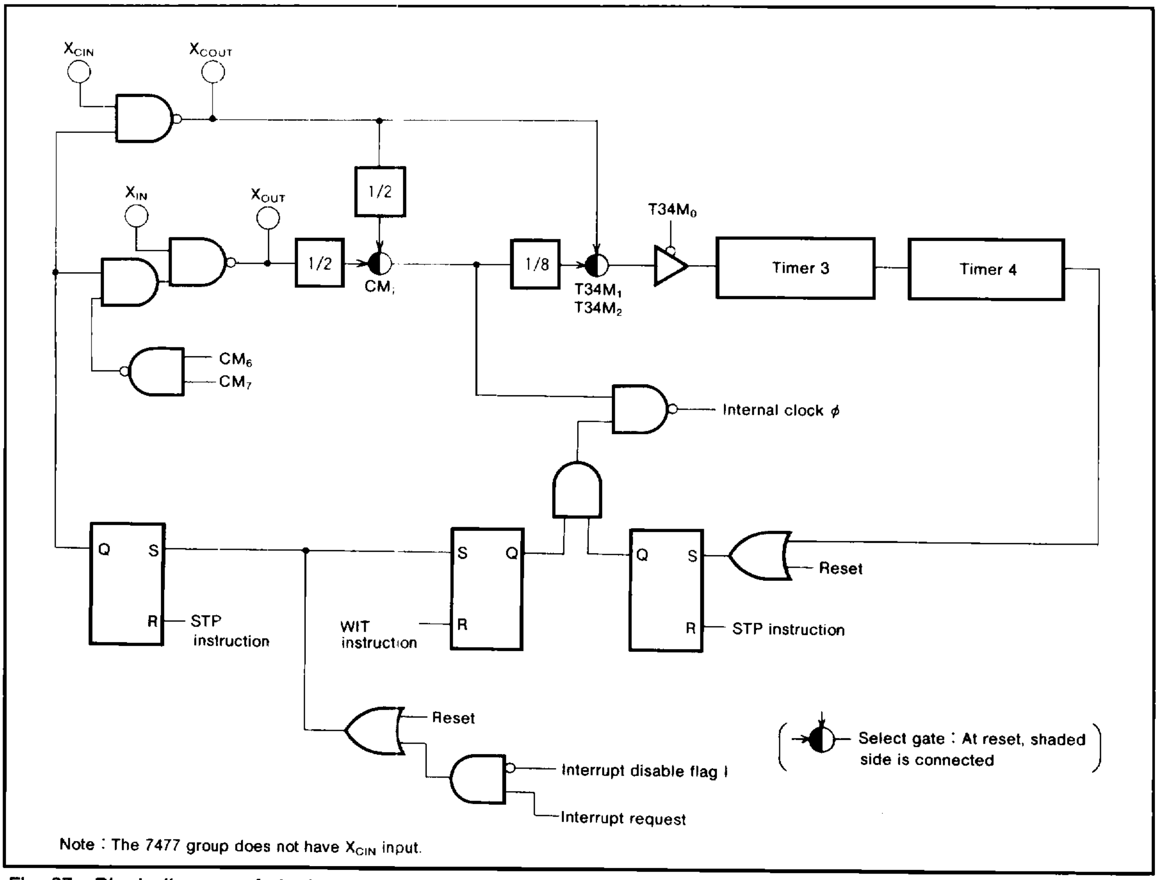


Fig. 27 Block diagram of clock generating circuit

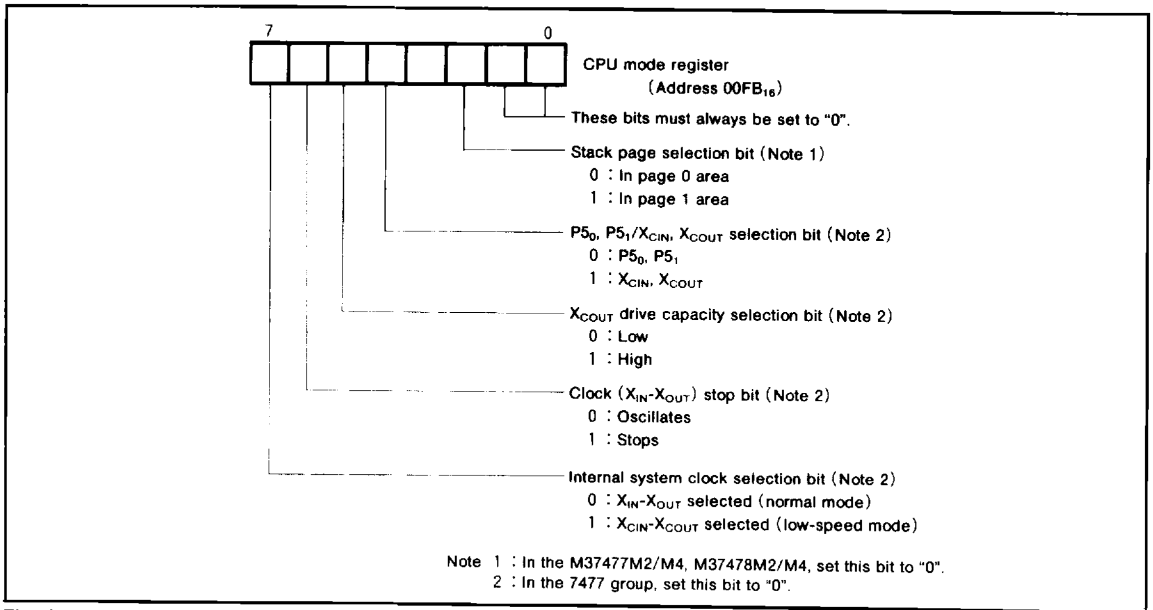
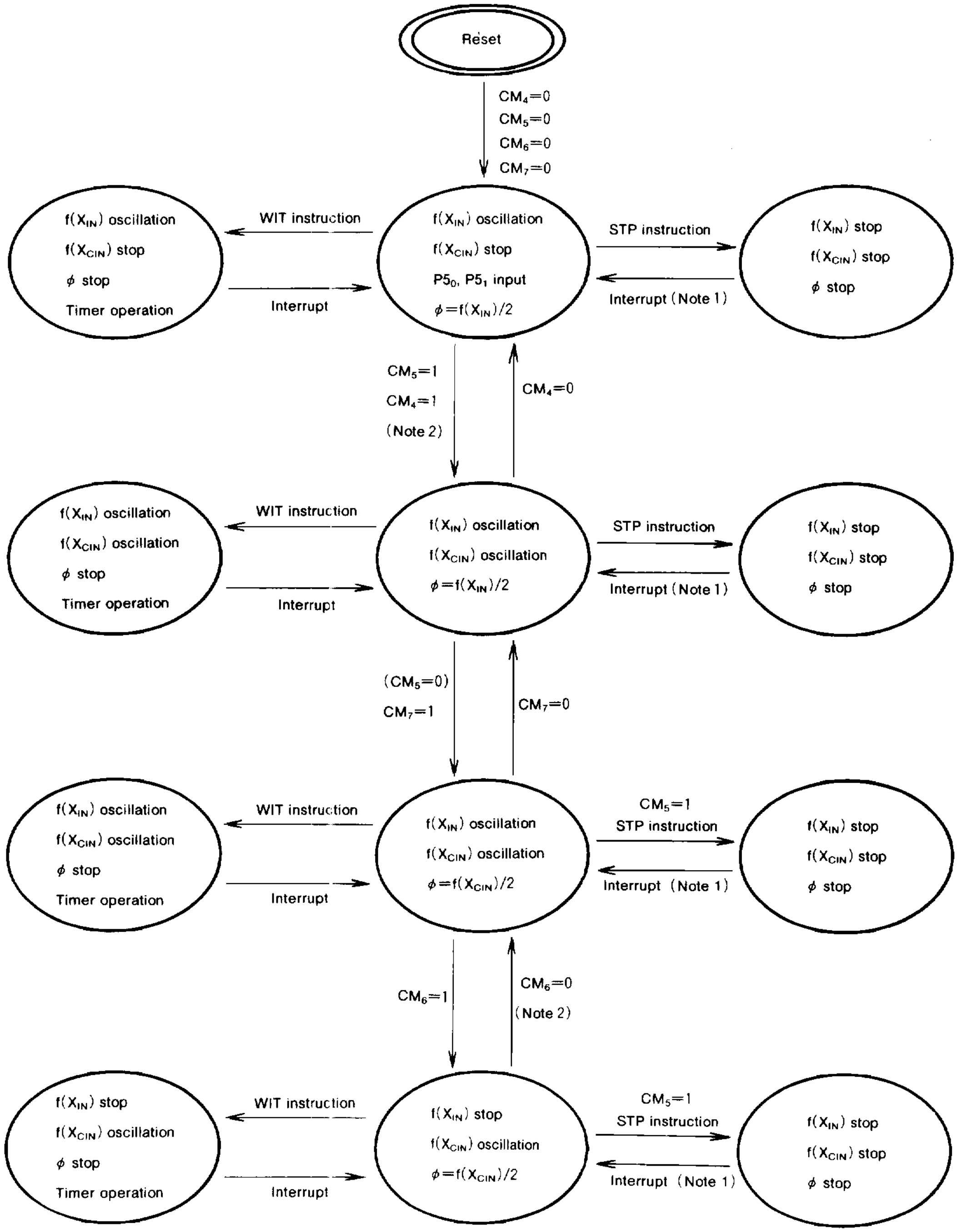


Fig. 28 Structure of CPU mode register



Note 1 : Latency time is automatically generated upon release from the STP instruction due to the connections of timer 3 and 4.

2 : When the system clock is switched over by restarting clock oscillation, a certain wait time required for oscillation to stabilize must be inserted by the program.

Fig. 29 Transition of states for the system clock.

<An example of flow for system>

Normal operation

Power on reset
↓
Clock X oscillation
↓
Internal system clock start (X → 1/2 → ϕ)
↓
Program start from $\overline{\text{RESET}}$ vector
⋮
[Normal program] ← Operating at $f(X_{IN})$
⋮

Operation on the clock function only

Clock for clock function X_C oscillation start (CM_4=1, CM_5=1)
↓
[Latency time for oscillation to stabilize (by software)] ← Operating at $f(X_{IN})$
↓
X_C clock power down (CM_5 : 1 → 0)
↓
Internal clock ϕ source switching X → X_C (CM_7 : 0 → 1)
↓
Clock X halt(X_C in operation)(CM_6=1)
↓
Internal clock halt(WIT instruction)
↓
→ Timer 4 (clock count) overflow
↓
Internal clock operation start (WIT instruction released)
⋮
[Clock processing routine] ← Operating at $f(X_{CIN})$
⋮
Internal clock halt (WIT instruction) (loops back to Timer 4 (clock count) overflow)

Return from clock function

Interrupts from INT_0, INT_1, $CNTR_0$/$CNTR_1$, timer 1, timer 2, timer 3, timer 4, serial I/O, key on wake up
↓
Internal clock operation start (WIT instruction released)
↓
Program start from interrupt vector
↓
Clock X oscillation start (CM_6=0)
↓
[Latency time for oscillation to stabilize (by software)] ← Operating at $f(X_{CIN})$
↓
Internal clock ϕ source switching (X_C → X)(CM_7 : 1 → 0)
⋮
[Normal program] → Operating at $f(X_{IN})$

RAM backup function

STP instruction preparation (pushing registers)

↓

Timer 3, timer 4 interrupt disable

↓

X/16 or X_C/16 selected for timer 3 count source; timer 3 overflow selected for timer 4 count source

↓

Timer 3, timer 4 start counting

↓

Values set to timer 3, timer 4 that do not cause timer 4 to overflow until STP instruction is executed

↓

Interrupt for return from STP enabled

↓

Timer 4 interrupt request bit cleared

↓

Clock X and clock for clock function X_C halt (STP instruction)

⋮

RAM backup status

Return from RAM backup function

Interrupts from INT_0, INT_1, $CNTR_0$/$CNTR_1$, timer 1, timer 2, serial I/O, key on wake up

↓

Clock X and clock for clock function X_C oscillation start

↓

Timer 4 overflow (X/16 or X_C/16→timer 3 →timer 4)

↓

Internal system clock start

↓

Program start from interrupt vector

⋮

Normal program

⋮

BUILT-IN PROM TYPE MICROCOMPUTERS PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Power source		Apply voltage of 2.7 to 5.5V to V_{CC} and 0V to V_{SS}.
AV_{SS}	Single-chip /EPROM	Analog power source		Ground level input pin for A-D converter. Same voltage as V_{SS} is applied. This pin is for M37478M2/M4/M8/E8-XXXFP only.
$\overline{RESET}$	Single-chip	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2μs or more (under normal V_{CC} conditions).
	EPROM	Reset input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open. Feedback resistor is connected between X_{IN} and X_{OUT}.
X_{OUT}		Clock output	Output	
V_{REF}	Single-chip	Reference voltage input	Input	Reference voltage input pin for the A-D converter.
	EPROM	Select mode	Input	V_{REF} works as $\overline{CE}$ input.
$P0_0-P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided.
	EPROM	Data input/output D_0-D_7	I/O	Port P0 works as an 8-bit data bus (D_0-D_7).
$P1_0-P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit. $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1. $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins R_XD, T_XD, S_{CLK}, $\overline{S_{RDY}}$, respectively.
	EPROM	Address input A_4-A_{10}	Input	$P1_1-P1_7$ works as the 7-bit address input (A_4-A_{10}). $P1_0$ must be opened.
$P2_0-P2_7$	Single-chip	Input port P2	Input	Port P2 is an 8-bit input port. This port is in common with analog input pins IN_0-IN_7.
(Note 1)	EPROM	Address input A_0-A_3	Input	$P2_0-P2_3$ works as the lower 4-bit address input (A_0-A_3). $P2_4-P2_7$ must be opened.
$P3_0-P3_3$	Single-chip	Input port P3	Input	Port P3 is a 4-bit input port. $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$.
	EPROM	Address input A_{11}, A_{12} Select mode V_{PP} input	Input	$P3_0$, $P3_1$ works as the 2-bit address input (A_{11}, A_{12}). $P3_2$ works as $\overline{OE}$ input. Connect to $P3_3$ to V_{PP} when programming or verifying.
$P4_0-P4_3$	Single-chip	I/O port P4	I/O	Port P4 is a 4-bit I/O port. The output structure is CMOS output. When this port is selected for input, pull-up transistor can be connected in units of 4-bit.
(Note 2)	EPROM	Address input A_{13}, A_{14}	Input	$P4_0$, $P4_1$ works as the higher 2-bit address input (A_{13}, A_{14}). $P4_2$, $P4_3$ must be opened.
$P5_0-P5_3$ (Note 3)	Single-chip	Input port P5	Input	Port P5 is a 4-bit input port and pull-up transistor can be connected in units of 4-bit. $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT}. If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin. Feedback resistor is connected between X_{CIN} and X_{COUT} pins.
	EPROM			Open.

Note 1 : Only $P2_0-P2_3$ (IN_0-IN_3) 4-bit for the 7477 group.
2 : Only $P4_0$ and $P4_1$ 2-bit for the 7477 group.
3 : This port is not included in the 7477 group.

EPROM MODE

The M37477E8, M37478E8 feature an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 2 lists the correspondence between pins and Figure 30 to 32 give the pin connection in the EPROM mode. When in the EPROM mode, ports P0, $P1_1-P1_7$, $P2_0-P2_3$, P3, $P4_0$, $P4_1$, V_{REF} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 2. Pin function in EPROM mode

	M37477E8, M37478E8	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	$P3_3$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports $P1_1-P1_7$, $P2_0-P2_3$ $P3_0$, $P3_1$, $P4_0$, $P4_1$	A_0-A_{14}
Data I/O	Port P0	D_0-D_7
$\overline{CE}$	V_{REF}	$\overline{CE}$
$\overline{OE}$	$P3_2$	$\overline{OE}$

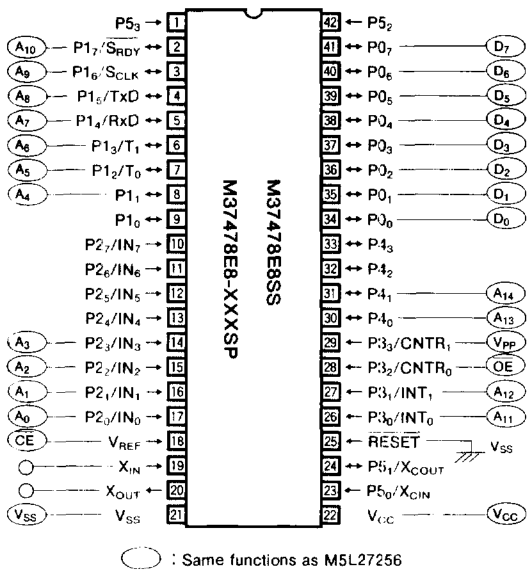


Fig.30 Pin connection in EPROM mode

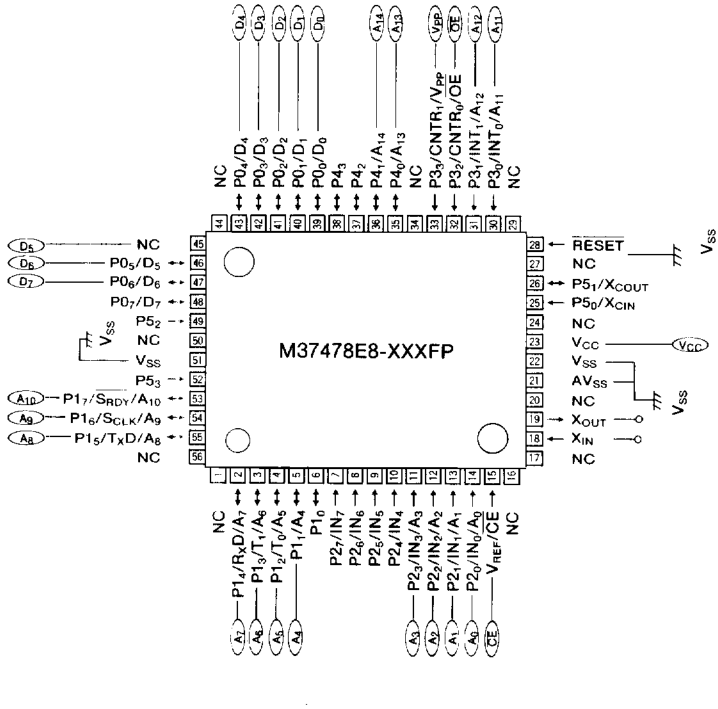


Fig. 31 Pin connection in EPROM mode

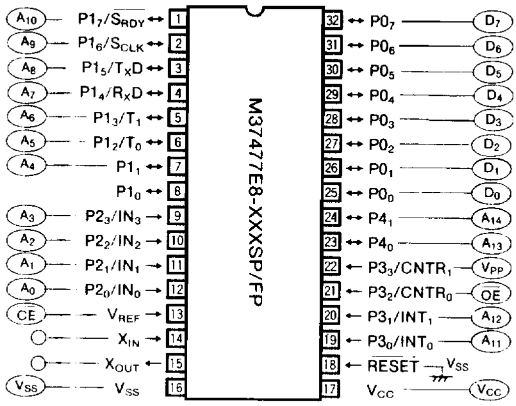


Fig.32 Pin connection in EPROM mode

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to "L" level. Input the address of the data ($A_0 - A_{14}$) to be read and the data will be output to the I/O pins $D_0 - D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 - A_{14}$, and the data to be written is input to pins $D_0 - D_7$. Set the $\overline{CE}$ pin to "L" level to begin writing.

Notes on Writing

When using a PROM programmer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

Erasing

Data can only erased on the M37478E8SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W • s/cm^2.

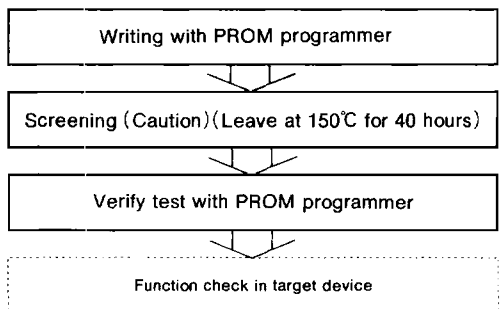
NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM programmer's power.

(4) For the programmable microcomputer (shipped in One Time PROM version), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Caution : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 3. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) The contents of the interrupt request bits are not modified immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

(3) To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instruction yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

(4) An NOP instruction must be used after the execution of a PLP instruction.

(5) Do not execute the STP instruction during A-D conversion.

(6) In the 7477 group, set bit 0, bit 1, and bit 3—bit 7 to "0" of the CPU mode register.

(7) Multiply/Divide instructions
The index X mode (T) and the decimal mode (D) flag do not affect the MUL and DIV instruction.
The execution of these instructions does not modify the contents of the processor status register.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ······································· EPROM 3 sets

M37477M2/M4/M8/E8-XXXSP/FP
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off	−0.3 to 7	V
V_I	Input voltage X_{IN}		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_3$, $P4_0$, $P4_1$ V_{REF}, $\overline{RESET}$		-0.3 to $V_{CC}+0.3$	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$, X_{OUT}		-0.3 to $V_{CC}+0.3$	V
Pd	Power dissipation	$T_a = 25$℃	1000 (Note)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 150	℃

Note: 500mW for M37477M2/M4/M8/E8-XXXFP.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃ unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	$f(X_{IN})=2.2V_{CC}-2.0$MHz	2.7		4.5	V
		$f(X_{IN})$=8MHz	4.5	5	5.5	
V_{SS}	Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$, $\overline{RESET}$, X_{IN}		$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$–$P2_3$, $P4_0$, $P4_1$		$0.7V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_3$		0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage $P2_0$–$P2_3$, $P4_0$, $P4_1$		0		$0.25V_{CC}$	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		$0.12V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}		0		$0.16V_{CC}$	V
$I_{OH(sum)}$	"H" sum output current $P0_0$–$P0_7$, $P4_0$, $P4_1$				−30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$–$P1_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$–$P0_7$, $P4_0$, $P4_1$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$–$P1_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$				−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$ (Note 1)				−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$ (Note 1)				10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)	$f(X_{IN})$=4MHz			1	MHz
		$f(X_{IN})$=8MHz			2	
$f(S_{CLK})$	Serial I/O clock input frequency S_{CLK} ($P1_6$) (Note 2) — Use as clock synchronous serial I/O mode	$f(X_{IN})$=4MHz			250	kHz
		$f(X_{IN})$=8MHz			500	
	Use as UART mode	$f(X_{IN})$=4MHz			1	MHz
		$f(X_{IN})$=8MHz			2	
$f(X_{IN})$	Clock input oscillation frequency (Note 2)	V_{CC}=2.7 to 4.5V			$2.2V_{CC}-2.0$	MHz
		V_{CC}=4.5 to 5.5V			8	

Note 1: The average output current I_{OH} (avg) and I_{OL} (avg) are the average value during a 100ms.
2: Oscillation frequency is at 50% duty cycle.

M37477M2/M4/M8/E8-XXXSP/FP
ELECTRICAL CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_1$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0$–$P0_7$, $P3_0$–$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6/S_{CLK}$	use as S_{CLK} input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$, $P4_1$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$–$P2_3$	V_I=0V, not use as analog input	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_2$, $P4_0$, $P4_1$	$V_I=V_{CC}$, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	$V_I=V_{CC}$	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$–$P2_3$	$V_I=V_{CC}$, not use as analog input	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	$V_I=V_{CC}$, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Power source current	At normal mode, A-D conversion is not executed	$f(X_{IN})$=8MHz, V_{CC}=5V		7	14	mA
			$f(X_{IN})$=4MHz, V_{CC}=5V		3.5	7	
			$f(X_{IN})$=4MHz, V_{CC}=3V		1.8	3.6	
		At normal mode, A-D conversion is executed	$f(X_{IN})$=8MHz, V_{CC}=5V		7.5	15	mA
			$f(X_{IN})$=4MHz, V_{CC}=5V		4	8	
			$f(X_{IN})$=4MHz, V_{CC}=3V		2	4	
		At wait mode.	$f(X_{IN})$=8MHz, V_{CC}=5V		2	4	mA
			$f(X_{IN})$=4MHz, V_{CC}=5V		1	2	
			$f(X_{IN})$=4MHz, V_{CC}=3V		0.5	1	
		At stop mode, $f(X_{IN})$=0, V_{CC}=5V	T_a=25℃		0.1	1	μA
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution				8	bits
—	Absolute accuracy				±3	LSB
t_{CONV}	Conversion time	V_{CC}=2.7 to 5.5V, $f(X_{IN})$=4MHz			25	μs
		V_{CC}=4.5 to 5.5V, $f(X_{IN})$=8MHz			12.5	
V_{VREF}	Reference input voltage		$0.5V_{CC}$		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

MITSUBISHI ELECTRIC

M37478M2/M4/M8/E8-XXXSP/FP, M37478E8SS ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to 7	V
V_I	Input voltage X_{IN}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_3$, $P4_0$—$P4_3$, $P5_0$—$P5_3$, V_{REF}, $\overline{RESET}$		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P4_0$—$P4_3$, X_{OUT}		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 150	℃

Note 1 : 500mW for M37478M2/M4/M8/E8-XXXFP.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{CC}	Power source voltage	f(X_{IN})=2.2V_{CC}−2.0MHz	2.7		4.5	V
		f(X_{IN})=8MHz	4.5	5	5.5	
V_{SS}	Power source voltage			0		V
AV_{SS}	Analog Power source voltage			0		V
V_{IH}	"H" input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P3_0$—$P3_3$ $\overline{RESET}$, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$—$P2_7$, $P4_0$—$P4_3$, $P5_0$—$P5_3$ (Note 1)		0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P3_0$—$P3_3$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$—$P2_7$, $P4_0$—$P4_3$, $P5_0$—$P5_3$ (Note 1)		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$—$P0_7$, $P4_0$—$P4_3$				−30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$—$P1_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$—$P0_7$, $P4_0$—$P4_3$				60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$—$P1_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P4_0$—$P4_3$				−10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P4_0$—$P4_3$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P4_0$—$P4_3$ (Note 2)				−5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P4_0$—$P4_3$ (Note 2)				10	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 3)	f(X_{IN})=4MHz			1	MHz
		f(X_{IN})=8MHz			2	
$f(S_{CLK})$	Serial I/O clock input frequency S_{CLK} ($P1_6$) (Note 2) — Use as clock synchronous serial I/O mode	f(X_{IN})=4MHz			250	kHz
		f(X_{IN})=8MHz			500	
	Use as UART mode	f(X_{IN})=4MHz			1	MHz
		f(X_{IN})=8MHz			2	
$f(X_{IN})$	Clock input oscillation frequency (Note 3)	V_{CC}=2.7 to 4.5V			2.2V_{CC}−2.0	MHz
		V_{CC}=4.5 to 5.5V			8	
$f(X_{CIN})$	Clock input oscillation frequency for clock function (Note 3, 4)			32	50	kHz

Note 1 : It is except to use $P5_0$ as X_{CIN}.
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the clock oscillation frequency for clock function should be $f(X_{CIN})<f(X_{IN})/3$.

M37478M2/M4/M8/E8-XXXSP/FP, M37478E8SS ELECTRICAL CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0 V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions			Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P4_0$−$P4_3$	V_{CC}=5V, I_{OH}=−5mA			3			V
		V_{CC}=3V, I_{OH}=−1.5mA			2			
V_{OL}	"L" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P4_0$−$P4_3$	V_{CC}=5V, I_{OL}=10mA					2	V
		V_{CC}=3V, I_{OL}=3mA					1	
$V_{T+}-V_{T-}$	Hysteresis $P0_0$−$P0_7$, $P3_0$−$P3_3$	V_{CC}=5V				0.5		V
		V_{CC}=3V				0.3		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V				0.5		V
		V_{CC}=3V				0.3		
$V_{T+}-V_{T-}$	Hysteresis $P1_6/S_{CLK}$	use as S_{CLK} input		V_{CC}=5V		0.5		V
				V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$−$P4_3$, $P5_0$−$P5_3$	V_I=0V, not use pull-up transistor		V_{CC}=5V			−5	μA
				V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor		V_{CC}=5V	−0.25	−0.5	−1.0	mA
				V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V		V_{CC}=5V			−5	μA
				V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$−$P2_7$	V_I=0V, not use as analog input		V_{CC}=5V			−5	μA
				V_{CC}=3V			−3	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)		V_{CC}=5V			−5	μA
				V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P3_0$−$P3_2$, $P4_0$−$P4_3$, $P5_0$−$P5_3$	V_I=V_{CC}, not use pull-up transistor		V_{CC}=5V			5	μA
				V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}		V_{CC}=5V			5	μA
				V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$−$P2_7$	V_I=V_{CC}, not use as analog input		V_{CC}=5V			5	μA
				V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)		V_{CC}=5V			5	μA
				V_{CC}=3V			3	
I_{CC}	Power source current	At normal mode, A-D conversion is not executed.	$f(X_{IN})$=8MHz	V_{CC}=5V		7	14	mA
			$f(X_{IN})$=4MHz	V_{CC}=5V		3.5	7	
			$f(X_{IN})$=4MHz	V_{CC}=3V		1.8	3.6	
		At normal mode, A-D conversion is executed.	$f(X_{IN})$=8MHz	V_{CC}=5V		7.5	15	mA
			$f(X_{IN})$=4MHz	V_{CC}=5V		4	8	
			$f(X_{IN})$=4MHz	V_{CC}=3V		2	4	
		At low-speed mode, T_a=25℃, $f(X_{IN})$=0, $f(X_{CIN})$=32kHz, X_{COUT} drive capacity is low, A-D conversion is not executed.		V_{CC}=5V		30	80	μA
				V_{CC}=3V		15	40	
		At wait mode.	$f(X_{IN})$=8MHz	V_{CC}=5V		2	4	mA
			$f(X_{IN})$=4MHz	V_{CC}=5V		1	2	
			$f(X_{IN})$=4MHz	V_{CC}=3V		0.5	1	
		At wait mode, T_a=25℃, $f(X_{IN})$=0, $f(X_{CIN})$=32kHz, X_{COUT} drive capacity is low		V_{CC}=5V		3	12	μA
				V_{CC}=3V		2	8	
		At stop mode, $f(X_{IN})$=0, $f(X_{CIN})$=0, V_{CC}=5V		T_a=25℃		0.1	1	μA
				T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation			2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7 to 5.5V, V_{SS}=AV_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy				±3	LSB
t_{CONV}	Conversion time	V_{CC}=2.7 to 5.5V, f (X_{IN})=4MHz			25	μs
		V_{CC}=4.5 to 5.5V, f (X_{IN})=8MHz			12.5	
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V